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INTERNATIONAL STANDARD

IEEE Std 2401™

Format for LSI-Package-Board interoperable design

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IEC 63055:2016-11(en) IEEE Std 2401-2015

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Contents

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FORMAT FOR LSI-PACKAGE-BOARD INTEROPERABLE DESIGN

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IEEE Standard Format for LSI-Package-Board Interoperable Design

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Abstract: A method is provided for specifying a common interoperable format for electronic systems design. The format provides a common way to specify information/data about the project management, netlists, components, design rules, and geometries used in Large-Scale Integrated Circuit-Package-Board designs. The method provides the ability to make electronic systems a key consideration early in the design process; design tools can use it to exchange information/data seamlessly.

Keywords: common interoperable format, components, design analysis, design rules, geometries, IEEE 2401™, large-scale integrated circuits, netlists, packages for LSI circuits, printed circuit board, project management, Verilog-HDL

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IEEE Introduction

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To deal with the increasing difficulty of design and the cost competitiveness of the global market, and to shorten the development term, innovative design methodologies should be implemented. It has been difficult to achieve the optimization of an entire set of large-scale integrated (LSI) circuits, packages, and board (LPB) using individual design processes for each LPB part.

One possibility for optimization is to have a certain section design the whole LPB; however, gathering knowledge and integrating the design environment of each LPB part is difficult. Dedicated professional technicians of individual LPB parts, who have the best knowledge and performance of their own part's design tools, intend to create design optimization by having proper interoperable information exchanges among all LPB parties. In order to achieve a design that optimizes the balance between cost and performance, information about and the results of design should be well shared among cooperating LPB design sections.

The Japan Electronics and Information Technology Industries Association (JEITA) LPB Interoperable Design Process Working Group (LPB-WG) was established to identify the solution. The LPB-WG intends to make a standard for an exchange format to make it easy to exchange information between each of the LPB design departments, so that optimal design will be carried out quickly.

The LPB interoperable design process has the following issues:

- Netlist not unified on each LPB
- Complexity of the representation of the relationship as a whole arrangement of the LPB
- Differences in how to give the design constraints, lack of design information, and many discrepancies in design rules.
- Databases not unified in each LPB, or among different vendors
- No unified terms

Various problems caused by these issues include the following:

- A large effort is required for conversion of formats.
- The occurrence of conversion errors and connection errors is difficult to detect because there is a lack of the information needed to do so.
- It takes a long time to gather information, resulting in a long period of design and analysis.
- It is difficult to make optimal design changes because the entire verification process is difficult.
- EDA tool cost increase because of additional development required to support multiple formats.
- It is time-consuming for designers to communicate their intentions in a way that others understand.

Based on this analysis, the LPB-WG has established an interface format that can address these issues.

As the one of the case studies of the LPB interoperable design process, the power distribution network (PDN) should be designed with information about the other LPB parts to reduce the noise (see Figure i).

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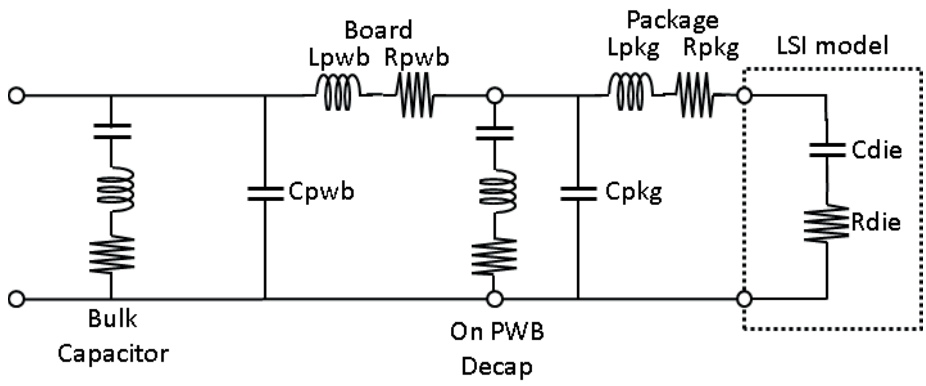

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Figure i—Power distribution network

Resonance is caused by a capacitance and inductance present in the various parts in the LPB PDN. Impedance at the resonant frequency will be extremely large. If each part of the overall LPB design is not accurately simulated in the PDN model, the power supply circuit cannot be correctly designed (see Figure ii).

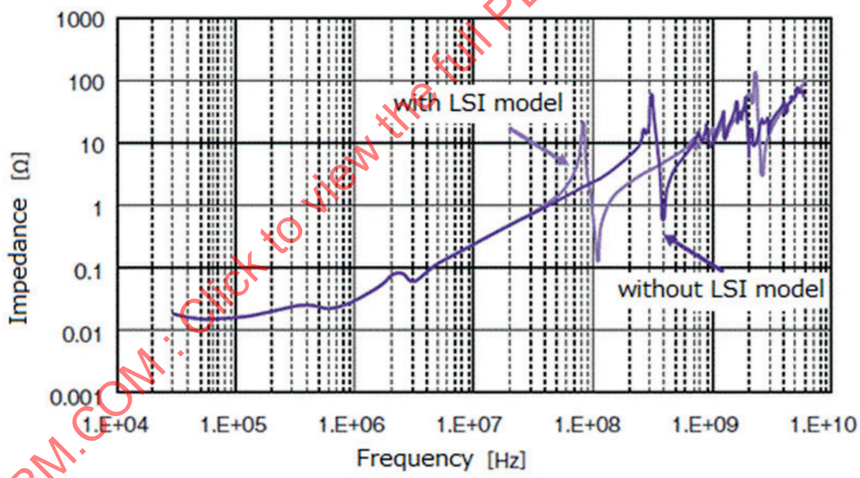

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Figure ii—Example of PDN impedance

In order to run properly, this simulation should align a variety of information, such as the circuit model of power distribution network (PDN) of LSI, shape information about the package and board, electrical parameters of materials, and models of the components. It is difficult to make an efficient design when the specification or format of the design information is different in each part of the LPB, and the necessary parameters are not shared. When the format of the interface methods and models of the simulation are not consistent, the setup time and the cost of design/verification are enormous, which has become a barrier to cooperation in LPB design. The LPB-WG was established in JEITA to explore ways to create a mutual LPB interface to enable a more efficient co-design environment.

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1. Overview

1.1 Scope

This standard defines a common interoperable format that will be used for the design of a) large-scale integration (LSI), b) packages for such LSI, and c) printed circuit boards on which the packaged LSI are interconnected. Collectively, such designs are referred to as" LSI-Package-Board" (LPB) designs. The format provides a common way to specify information/data about the project management, netlists, components, design rules, and geometries used in LPB designs.

1.2 Purpose

The general purpose of this standard is to develop a common format that LPB design tools can use to exchange information/data seamlessly, as opposed to having to work with multiple different input and output formats.

1.3 Key characteristics of the LSI-Package-Board Format

LPB format will facilitate the exchange of design information. This functionality provides the ability to plan the entire design at an early stage. In effect, post-design analysis will be possible throughout the entire

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LPB design process. Analysis of each part of the design can be examined in relation to all other parts of the design, to determine the optimal point to give feedback for appropriate design changes throughout the LPB. This will promote the overall optimization of the design process.

The LPB Format is constructed out of the following five formats (see Figure 1):

a) Project Manage (M-Format)
b) Netlist (N-Format)
c) Component (C-Format)
d) Design Rule (R-Format)
e) Geometry (G-Format)

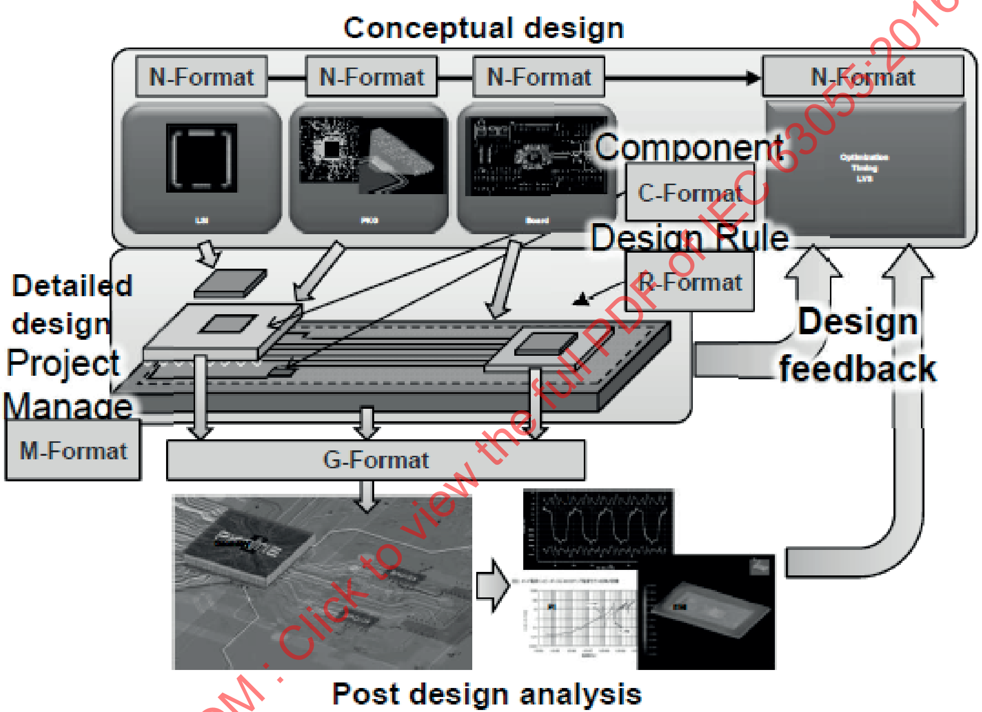

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Figure 1—LPB Format

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Design time can be shortened by using the LPB Format. Traditionally, design starts immediately after separate planning for each individual component of the LPB. Therefore, information exchange among the separate design processes is limited. Trying to adjust the detailed design of one component to the detailed design of another component makes the entire design period take longer. Optimization also tends to be a separate process for each component of the LPB. By using the LPB Format for distributing information, each LPB technician will be able to have the same understanding of the challenges at an early stage. As a result, adjustments at the conceptual design stage can be made, before detailed designs are developed. By making clear the overall LPB product specifications, the design target can be decided, and so the duration of individual designs can be shortened. Use of the LPB Format also helps to reduce the number of design iterations, because the design quality is enhanced. The designers can collect all information for simulation

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using the LPB formats, thereby reducing production time. The LPB Format can enable the entire analysis easily, so that sufficient verification can be done and the quality of the products can be improved. As a result, the period of adjustment in the set can be shortened and the time to market can be accelerated. With the LPB Format, the design method for one product can be applied to the design environment for next product in development.

1.4 Contents of this standard

The organization of the remainder of this standard is as follows:

- Clause 2 provides references to other applicable standards that are presumed or required for this standard.
- Clause 3 defines terms and acronyms used throughout the different specifications contained in this standard.
- Clause 4 describes the concepts of the LPB Format.
- Clause 5 describes the language basics for the LPB Format and its commands.
- Clause 6 describes common elements in the M-Format, C-Format, and R-Format.
- Clause 7 describes the M-Format.
- Clause 8 describes the C-Format.
- Clause 9 describes the R-Format.
- Clause 10 describes the N-Format.
- Clause 11 describes the G-Format.

2. Normative references

The following referenced documents are indispensable for the application of this document (i.e., they must be understood and used, so each referenced document is cited in text and its relationship to this document is explained). For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments or corrigenda) applies.

IEEE Std 1364™, IEEE Standard for Verilog Hardware Description Language.[1,2]

3. Definitions, acronyms, and abbreviations

3.1 Definitions

For the purposes of this document, the following terms and definitions apply. The *IEEE Standards Dictionary Online* should be consulted for terms not defined in this clause.[3]

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antipad: The clearance **hole** between a **via** and a no-connect metal layer, mainly used on the printed circuit **board** and LSI **package**. The shape of the antipad is mainly determined by the limit on the printed circuit board or LSI package manufacturing and is defined by the **padstack** in the R-Format file.

ball grid array (BGA) package: A type of surface-mount **package** with one face covered (or partly covered) with **solder balls** arranged in a grid pattern.

ball: *See:* **solder ball**.

board: The printed circuit board or printed wiring board.

bonding finger: The metal electrode on the surface of an LSI **package**. It connects the **bonding wire** to the routing pattern on the LSI package. In LPB Format files, the shape of the bonding finger is defined by the **padstack** in the C-Format file.

bonding wire: A metal wire for connecting the **die** and **bonding finger**. In LPB Format files, the shape of the bonding wire is defined in the R-Format file.

clock: The signal used in a synchronous circuit. All synchronous circuits use a clock signal to synchronize different parts of the circuit. In most cases, the part is register or flip-flop. The clock is distributed from a single source to registers or flip-flops and is required to arrive at all such parts at the same time

common mode impedance: The impedance of a single transmission line when the two lines in a pair are driven with signals of the same amplitude and same polarity. Common (even) and differential (odd) modes are the two main modes of propagation of the signal through a coupled line pair.

component: A physical and logical construction having inputs to outputs. LSI package or semiconductor chips and passive parts such as capacitors and connectors are called components.

component hole: A **hole** used for the attachment of component terminations to the printed **board** as well as for any electrical connection to the conductive pattern. *See also:* **hole**.

delay: The time interval between a step function change of the input signal level and the instant at which the magnitude of the output signal passes through a specified value that is close to its initial value. The switching time of the transistor and the propagation time of the signal through wiring.

die: A separated part (or whole) of a wafer intended to perform a function or functions in a device. A small block of semiconducting material, on which a given functional circuit is fabricated.

differential mode impedance: The impedance of a single transmission line when the two lines in a pair are driven with signals of the same amplitude and opposite polarity. Common (even) and differential (odd) modes are the two main modes of propagation of the signal through a coupled line pair.

differential signal: Differential signaling. A method of transmitting information electrically with two complementary signals sent on two paired wires, called a differential pair.

drill: The drill to be used when drilling the **via** hole connecting the layers of a multilayer printed circuit **board**.

driver: *See:* **sender**.

finger: *See:* **bonding finger**.

flipchip pad: The contact pad of the **flipchip** surface.

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flipchip: A chip that is flipped over so that its metal wiring faces down in order to mount the chip to external circuitry (e.g., a circuit board or another chip or wafer).

guard shield: A barrier or enclosure provided for mechanical protection, which may also have the function of a screen, called a "GND shield" when put on a ground (GND) conductor. Its purpose is to limit the electromagnetic interference from other signals.

hole: Used for the conductive connection between each layers and for mounting components. *See also:* **component hole**, **landless hole**, **mounting hole**, **plated-through hole,** and **via hole**.

inout: A **port** having the function of both input and output**.** It is an input port where electromagnetic energy or signals may be received from an external circuit or device**.** It is an output port where electromagnetic energy or signals may be supplied to an external circuit or device**.**

land: The conductive pattern used for joining and connecting parts, the conductive pattern for surface mount pads and hole-mounted components, and the conductive pattern that covers a via hole.

landless hole: A **plated-through hole** without **land**. *See also:* **hole**.

line: A device connecting two points for the purpose of conveying electromagnetic energy between them. Electromagnetic energy may be extracted from or supplied to a line at an intermediate point. Examples of lines are two-wire line, polygon line, coaxial line, and waveguide.

mounting hole: A **hole** used for the mechanical mounting of a printed **board** or for mechanical attachment of components to the printed board. *See also:* **hole**.

net: The relative position of the ideal elements representing an electric network. The label in between interconnection of terminals. Although it is defined on the same hierarchy, there are also cases that indicate the connection regardless of hierarchy (for example, global net/definition).

package mold: Protection of an LSI chip by resin against stress, external force, water, static electricity, and foreign substances. A package mold contains resin, silica, carbon, and flame retardant material.

package substrate: The same as that of a printed circuit board. It carries LSI and electrically connects **solder balls** with LSI.

package: An enclosure for one or more chips, film elements, or other components, that allows electrical connection and provides mechanical and environmental protection. Types of packages include quad flat package (QFP), ball-grid array (BGA), wafer-level chip-scale package (WLCSP), multi-chip module (MCM), package on package (PoP), etc.

pad: A metal electrode on the surface of a semiconductor device, LSI package, or printed circuit **board**.

padstack: The combination of layers that constitute a **pad**.

physical design rule: A series of parameters provided by semiconductor manufacturers that enable the designer to verify the correctness of a mask set. A design rule set specifies certain geometric and connectivity restrictions to ensure sufficient margins to account for variability in semiconductor manufacturing processes, so as to ensure that most of the parts work correctly.

pin: A contact element intended to make electric engagement on its outer surface for mating with the inner surface of another contact element.

plated-through hole: A **hole** in which metal is deposited on the wall. *See also:* **hole**.

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port: Access to a device or network where electromagnetic energy or signals may be supplied or received, or where the device or network variables may be observed or measured.

NOTE—An example of a port is a terminal pair.[4]

power domain: A collection of instances that are treated as a group for power-management purposes. The instances of a power domain typically, but do not always, share a primary supply set. A power domain may also have additional supplies, including retention and isolation supplies.

receiver: A device that receives signals for interpretation and action.

reference point: A point of reference that is used for representing the coordinates.

sender: A device that generates and terminates signals. *Syn:* **driver**.

single-ended signal: A signal used for single-ended signaling, which is the method of transmitting signals over electrical connections. One electrical connection carries a varying voltage that represents the signal.

skew: A variation of a delay time by propagation of a signal, or an amount of gaps of the delay time between a reference signal and an object signal.

solder ball: A spherical solder that is used in the LSI package of a **BGA** type and provides the contact between the **package** and the printed circuit **board**. The **pins** of the BGA package are placed in a grid pattern. Balls are mounted on each pin and used to solder the BGA to the printed circuit board. The internal circuit in a BGA exchanges signals and power with an external circuit on a printed circuit board through the ball. The shape of the ball is defined in the R-Format file.

stacked via: A structure that places a **via** on another via. *See also:* **via**.

sub-circuit: A sub-circuit expresses a specific circuit as one unit.

terminator: A device fitted to the end of a cable to ensure electrical connection with other parts of the system and to maintain the insulation up to the point of connection.

typ: An abbreviation of “typical,” used to express a representative or standard value.

via hole: The conduction connectivity made through a **hole** in between layers. *See also:* **hole**.

via: One of the conductive parts forming a contact in between layers.

void: A **hole** or cutout on a plane.

3.2 Acronyms and abbreviations

ASCII	American Standard Code for Information Interchange
BGA	ball grid array
CPIP	Chip-Package Interface Protocol
DC	direct current

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DDR	double data rate
DDR-SDRAM	double data rate synchronous dynamic random-access memory
DEF	Design Exchange Format
DXF	Drawing Exchange Format
EDA	electronic design automation
EMI	electromagnetic interference
GDS (GDS II)	Graphic Database System
GND	ground
HDL	hardware description language
ICEM	integrated circuit emission model
ICIM	integrated circuit immunity model
IEC	International Electrotechnical Commission
I/O	input output
IBIS	Input/output Buffer Information Specification
IC	integrated circuit
JEDEC	Joint Electron Device Engineering Council
JEITA	Japan Electronics and Information Technology Industries Association
LPB	LSI, package, and board; LSI-Package-Board
LPB-WG	LPB interoperable design process working group
LSI	large-scale integration
MD5	message digest algorithm 5
NG	no good
PCB	printed-circuit-board (adjective)
PCIe	Peripheral Component Interconnect Express
PKG	package
PKI	public key infrastructure
POP, PoP	package on package
PWB	printed wiring board

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RMS	root mean square
Si2	Silicon Integration Initiative
SMA	subminiature version A
SoC	System on Chip
SPICE	Simulation Program with Integrated Circuit Emphasis
VHDL	Very High Speed Integrated Circuits Hardware Description Language
XML	Extensible Markup Language
Xtal	crystal

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4. Concept of the LPB Format

4.1 Technical background

The design margin for timing and noise is decreasing due to the higher speed of systems and the low voltage of the interface and power supply. Also, balancing design for both cost and performance is increasingly becoming important for cost competitiveness. In a conventional design, the LSI, package, and board (LPB) are designed with margin in accordance with individual design guidelines. However, it becomes difficult to provide design guidelines for each LPB part separately with the decreased design margin. Therefore, deciding the design target needs the cooperation of the designers of each part of the LPB. In other words, the innovation of deciding design guidelines by using simulation technology is needed in the system design process. To perform this task, a rapid and accurate simulation environment is necessary.

4.2 Conventional design

In conventional design, LPB design and sign-off analysis were performed for each design criterion. In other words, only partial optimization was done, so whole-system optimization and analysis was not performed at the initial design stage. The result was a lack of observation of physical phenomena throughout the whole system, appropriate design changes on each design site separately, and excessive estimation for design margin. These significantly influenced the quality and cost of the final product.

4.3 Common problems at the design site

4.3.1 Misunderstanding among designers

Misunderstanding among designers can occur when different designers perceive the same word to have different meanings, designers use the different words to describe the same phenomenon, and designers have different subjectivities, such as viewing the design from the top or bottom. These cases occur even if designers are in the same office, with the result that many designers have a bitter experience.

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4.3.2 Lack of information for system design

Limitations and design margins among the LSI, package, and board may not be assumed at the time of the design of the individual components. Also designers may face big obstacles after connecting individual components because they are uncertain about the limitations and margins of the others. For example, designing the package or board (wiring) will be difficult because of lack of information about the LSI pad assignment, the package ball assignment, and the part location on the board.

4.3.3 Waste of time that should be used for design

Because input and output formats are different for each electronic design automation (EDA) vendor, in some cases the designer needs to convert the format at the time of the delivery of the data from the different EDA vendors. Problems occur when the designer lacks information at the time of format conversion and has to make up for its lack later. In addition, the pin name and net names may be different for every LSI circuit, package, and board. The designer needs to adjust those data and spend painful time in correction.

4.4 Concept of LPB interoperable design

Interoperable design is the solution method for the problems with using conventional individual design methods for each LPB part. It is defined as the style that each LPB section uses to cooperate and design. At first, the designer makes minimum design guidelines to satisfy the product's performance standards by designing through the whole LPB using the interoperable design. After that, the designer designs each part individually in accordance with the design guidelines. After each individual design is completed, the designer performs a simulation for integrating that part with the whole LPB, confirms the performance of all products, and provides feedback on the designs for all other parts accureately.

4.5 Value creation by LPB interoperable design

4.5.1 Effects of LPB interoperable design

LPB interoperable design is an appropriate method of design throughout a whole system for signal integrity and power integrity among LPB components. This technology is a solution for the problems discussed in 4.3. Use of LPB interoperable design makes it is possible to get the effect described in the following subclauses.

4.5.2 Reduction of development cost and time by design flow without iteration

When the designer finally connects the parts designed by partial optimization, an unexpected lack of design margin sometimes occurs. The designer then needs to discover which part of the LPB is causing the margin bottleneck. As a result, the designer may not only spend a lot of time but also need additional recovery costs for creating the needed design margin. In such cases, it is possible to reduce the development cost and time by starting LSI design, package design, and board design with each designer sharing information and cooperating from the point that the LSI design begins. Figure 2 compares conventional design flow and LPB interoperable design flow. The LPB interoperable flow reduces development costs and time.

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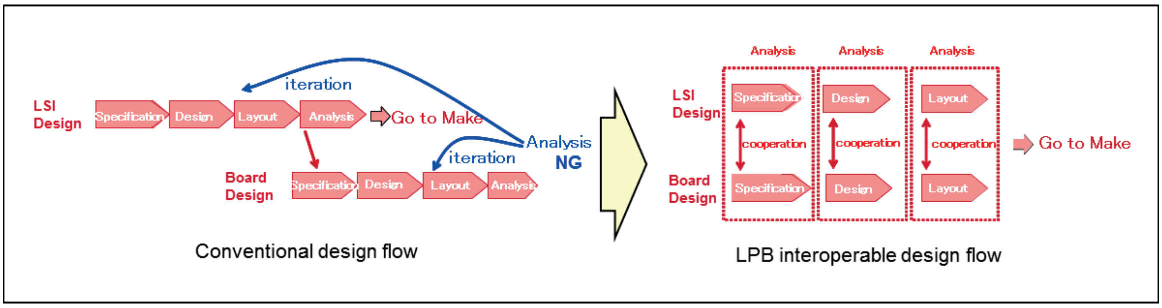

Figure 2—Conventional design flow versus LPB interoperable design flow

4.5.3 Reduction of system total cost

In conventional design, because a designer designs each part of the LSI, package, and board separately with separate, individual margins, the design margin of the product as whole system sometimes becomes excessive when the parts are finally connected. It is possible to reduce the total cost using LPB interoperable design because the design margin for the whole design is controlled and held in total, including reduction of the number and cost of the parts used in the design. Figure 3 compares the design margins of conventional design flow and LPB interoperable design flow.

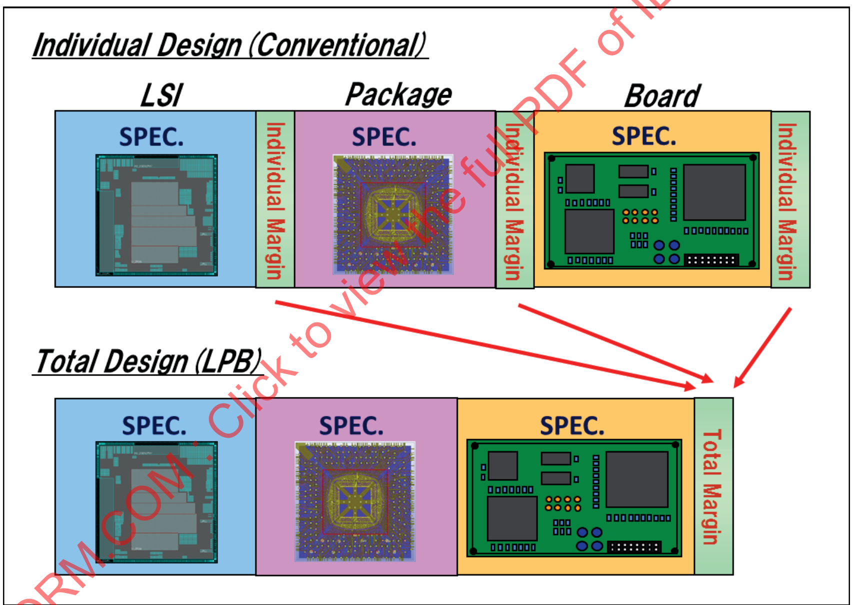

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Figure 3—LPB interoperable design can control design margin

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4.6 LPB Format

LPB Format solves the problems in conventional design methodologies, improves product quality, and reduces design time. LPB Format is a common language for describing the information required for design and verification. It reduces the preparation time of EDA tools in design teams. Furthermore, LPB can enable the sharing of ideas beyond the design teams. It can become a medium for information distribution

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in the supply chain. It prevents misunderstanding of design information and improves the information flow in the whole industry. As the result, quality, cost, and delivery time (QCD) will be improved.

4.7 Summary of LPB Format files

4.7.1 General

Figure 4 shows one example of how design information is exchanged using the LPB Format. In this example, three types of designers exists: the LSI designer, the package designer, and the board designer. All designers exchange design information using LPB Format standard files. By unifying the notation of the files for exchanging design information, it is possible to prevent misunderstandings and to automate the design tool settings.

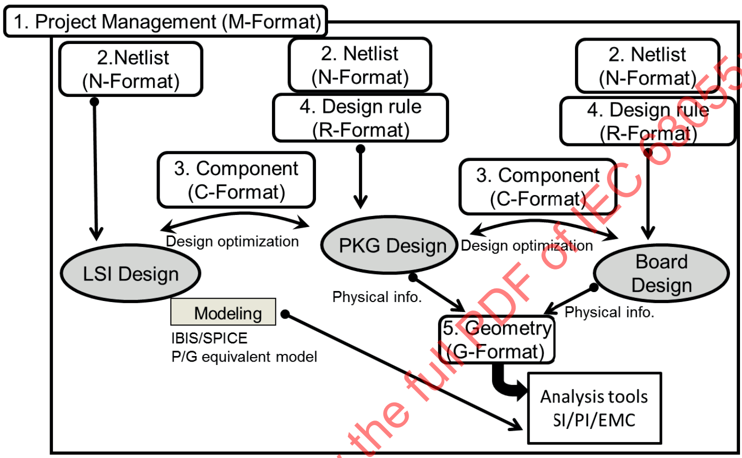

Figure 4—Example of exchanging design information using the LPB Format

4.7.2 C-Format

The first purpose of C-Format is to give a unified notation to the outer specifications for parts, such as the LSI, package, socket, and so forth. The outer specification is the information needed in order to use the parts, as follows:

— Physical shape of the parts

— Name and type of signal to be input to and output from the parts

— Input/output (I/O) specification, such as the physical shape and position of pins, or swappable pin definitions

— Design constraints, such as the upper limit of the delay or skew

— Design specifications, such as the input impedance of pins or power consumption

By unifying the notation with C-Format, it is possible to exchange information without misunderstanding. For example, a board designer should understand the specifications delivered from several LSI vendors and should set up the design tools based this understanding. Human error may occur during this process if the specifications are described by each vendor's own notation. Using C-Format instead of vendors' own notations, it is possible to set up the design tool automatically and to prevent human error due to

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misunderstanding. Figure 5 shows an example of the information flow of LSI specifications using C-Format. The LSI specifications are all provided by C-Format even if the vendors are different. The board designer can understand the specifications by reading only one notation, and design tools can automatically set up themselves by entering C-Format.

Figure 5—Example of information flow of LSI specifications using C-Format

Unified notation also smoothly circulates information about specification changes. Figure 6 shows an example of interoperable design flow. A board designer and an LSI designer are collaborating. The information about the pin assignment of the LSI package is provided by the LSI designer. When the board designer want to change the pin assignment of the LSI package, he or she modifies the provided C-Format file and returns it to the LSI designer. The use of C-Format prevents misunderstanding about the specification change and prevents human error that can occur due to specification changes.

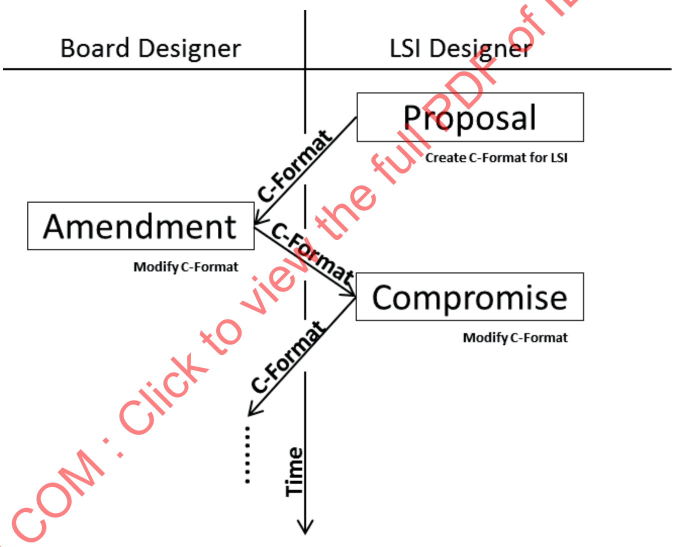

Figure 6—Example of interoperable design flow with C-Format

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The second purpose of C-Format is to provide a unified interface to a simulation model such as a Simulated Program with Integrated Circuit Emphasis (SPICE) netlist, Input/output Buffer Information Specification (IBIS), S-parameters, etc. C-Format wraps these simulation model files and gives cross-references between the nodes of the simulation model and the physical ports of the parts. Simulation tools can plug in the simulation model automatically by entering the wrapped model file. Figure 7 shows an example of exchanging simulation models. Model files are provided with the C-Format file.

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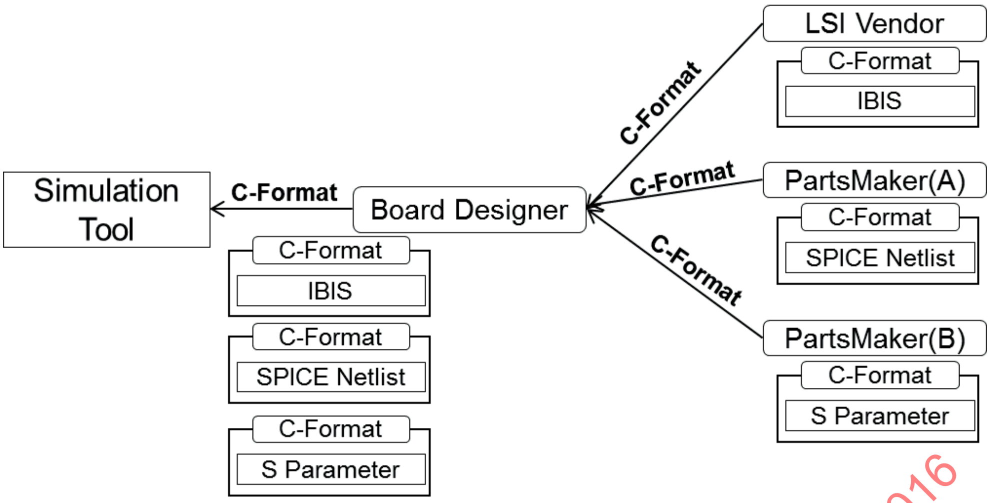

Figure 7—Example of exchanging simulation models with C-Format

The third purpose of C-Format is to provide connection points to merge multiple layout data. C-Format wraps layout data files, such as Graphic Database System (GDS) II, and gives cross-references between ports in the C-Format file and objects in the layout data file. For example, when the C-Format file wraps a GDS II file, ports in C-Format are associated with the coordinates/layers in the GDS II file. When the C-Format file wraps a G-Format file, the ports in the C-Format file are associated to the pin in the G-Format file. This feature can be used to merge two or more layout data designed by different design houses. Such situations can occur when the board designer wants to analyze the board with package layout data. The board designer receives the wrapped package layout data from the package designer and enters it in the analysis tools. The analysis tools can find the connection points using the cross-references defined in the C-Format file and merge the layout data of the printed circuit board and the package.

The fourth purpose of C-Format is to support the floorplan of the printed circuit board and package. C-Format includes placement information about the parts. This feature can be used to communicate the floorplan information from system designer to board designer. Figure 8 shows an example of design flow when the system designer requests a printed circuit board design from the board designer. At the beginning of the work, the printed circuit board designer can set up the design tools based on the provided C-Format file. By unifying the notation of the floorplan, it is possible to exchange floorplan information without misunderstanding, and to set up the design tool automatically.

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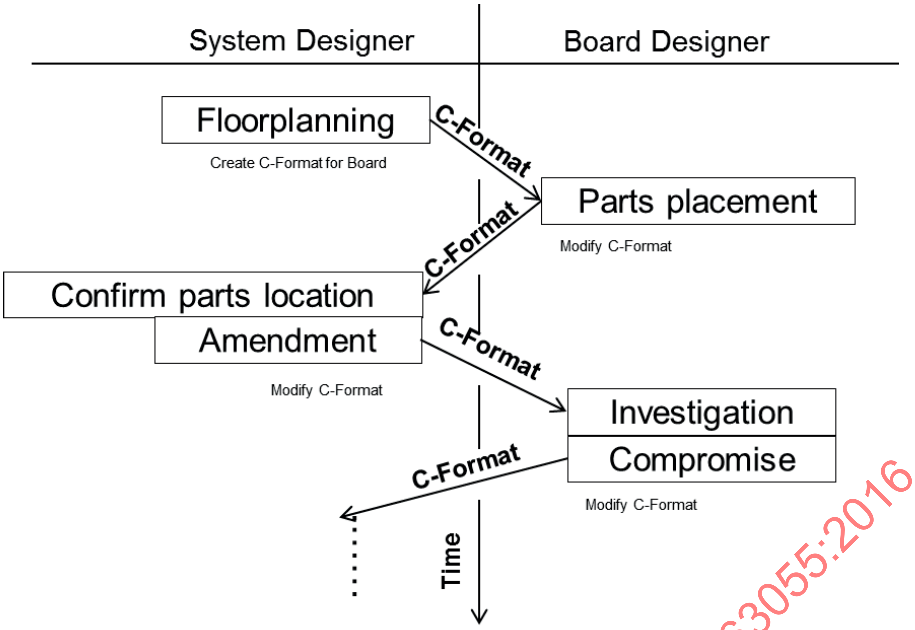

Figure 8—Example of design flow between system designer and board designer

4.7.3 R-Format

The first purpose of R-Format is to unify the notation of the design rules of the printed circuit board and the package. The following design rules are defined in R-Format:

- Layer stackup of the package and the printed circuit board
- The thickness of the conductive layer/insulating layer
- The materials used for each layer
- The material parameters, such as conductivity, dielectric constant, or loss tangent
- Line width and line space
- Via spacing
- Shape of vias

Normally, manufacturers of printed circuit boards and packages provide the design rules using their own notations. The designer has to understand the design rules described in several notations and set up the design tools, with the risk that human error may occur. However, using a unified notation such as R-Format makes it possible to set up the design tool automatically and to prevent misunderstanding. Figure 9 shows an example of exchanging design rules using R-Format. All manufactures provide design rules using the R-Format unified notation. Design tools can set up themselves automatically by entering R-Format.

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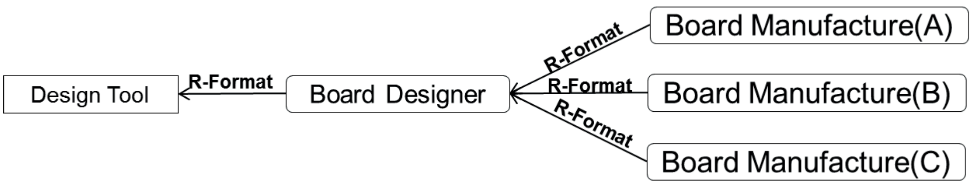

Figure 9—Example of exchanging design rules with R-Format

The second purpose of R-Format is to define the physical design constraints of the printed circuit board and the package. Where, the physical design constraints means that the height limitation of mounted parts and non-default design rule area.

4.7.4 G-Format

The purpose of G-Format is to unify the notation of the layout data of the layer stack-up structure, such as the printed circuit board or package. It is possible to exchange the layout data seamlessly between analysis tools and layout tools by the unified notation of the layout data. The G-Format file includes the following geometric information:

- Printed circuit board
- Layer stackup and physical parameters of the material
- Shape and location of the mounted parts
- Shape and location of the pins
- Route or pattern of the nets
- Shape and location of the vias
- Shape of the bonding wires

Figure 10 shows an example of exchanging layout data using G-Format. Analysis tools can set up by only entering G-Format if all layout tools output G-Format file.

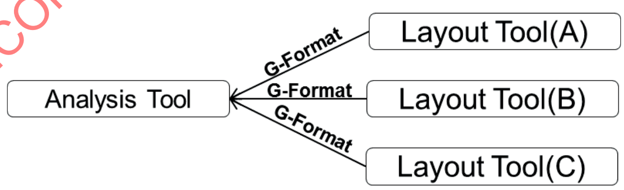

Figure 10—Example of exchanging layout data with G-Format

4.7.5 N-Format

The purpose of N-Format is to unify the notation of the netlist that is used to design the printed circuit board and the package, where “the netlist” means the connectivity information between parts that are

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mounted on a printed circuit board or package. N-Format conforms to Verilog hardware description language (HDL) (IEEE Std 1364[5]) and adds keywords to identify power and ground nets. Unifying notation of the netlist makes it possible to exchange the netlist seamlessly between circuit design tools and layout tools. For example, when the circuit designer orders the board design from the board designers, the designers should exchange the netlist.

If the netlist is represented using several notations, there is a risk that human error may occur when entering the connectivity between parts into the design tools. However, by using the unified notation for netlist, it is possible to prevent human errors when setting up the design tools because all design tools can set up the connectivity between the parts by supporting only one notation for the netlist file. Figure 11 shows an example of design flow using the N-Format file. Circuit modification is exchanged using N-Format.

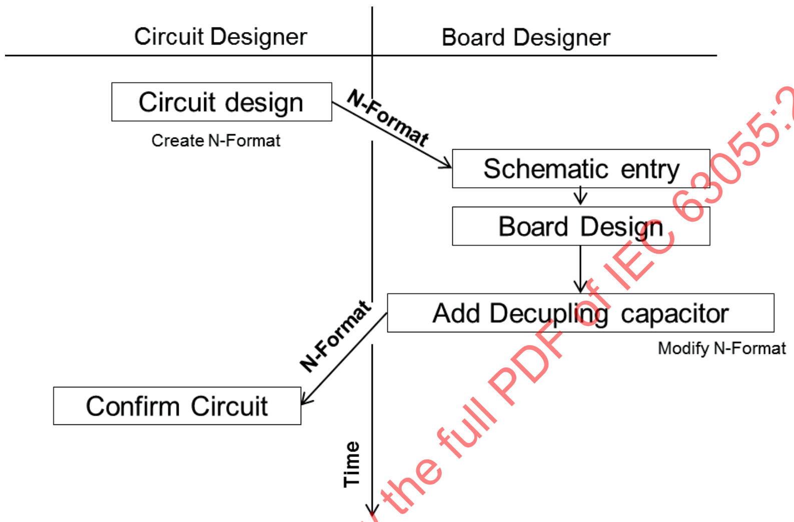

Figure 11 —Example of design flow with N-Format

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4.7.6 M-Format

LPB Format files are continuously updated in accordance with the design progress. The purpose of M-Format is to manage the version of each file to prevent errors when exchanging LPB Format files.

5. Language basics

5.1 General

This subclause describes the conventions used in the syntax definitions of the LPB M-Format, C-Format, and R-Format.

[5] Information on references can be found in Clause 2.

5.2 Typographic and syntax conventions

The following list describes the syntax conventions:.

`text`

The `monospace` font is used to indicate the attributes or elements that shall be typed literally.

`italic`

The *`italic`* font is used to indicate the user-defined information for which shall be substituted a name or value.

|

Vertical bars separate possible choices for a single attribute or element. They take precedence over any other character.

[ ]

Brackets denote optional attributes or elements. When used with vertical bars, they enclose a list of choices.

[ ]…

Brackets followed by three dots indicate that there shall be specified zero or more attributes or elements. When used with vertical bars, they enclose a list of choices.

{ }…

Braces followed by three dots indicate that there shall be specified one or more attributes or elements. When used with vertical bars, they enclose a list of choices.

…

Three dots indicate that the previous value could be repeated.

All of the strings in the M-Format, C-Format, and R-Format are case sensitive.

NOTE—All code examples in this standard are written in monospace font.

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6. Common elements in M-Format, C-Format, and R-Format

6.1 General

This clause provides commonly used elements in M-Format, C-Format, and R-Format.

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6.2 The <header> element

6.2.1 General

The `<header>` element defines the management information of the M-Format, R-Format, and C-Format files.

```
<header
            project="project_name"
            design_revison="revision_number"
            [date="date"]
            [author="owner_of_this_document"]
            [email="email_address"]
            [company="company_name"]
            [comment="any_comment"]
/>
```

By processing the `<header>` element, you can get the project name (`project`), creation date (`date`), information about the author (`author`, `email`, and `company`), and a control number (`design_revision`).

6.2.2 Attribute definitions

The attributes of the `<header>` element are defined as follows.

`project`

This attribute specifies the name of the project. All LPB Format files in a project shall have the same project name.

`design_revision`

This attribute specifies the revision number of each LPB Format file. The revision number shall be increased appropriately when modifying the LPB Format file.

`date`

This attribute specifies the creation or modification date of the LPB Format file.

`author`

This attribute specifies the name of the author of the LPB Format file.

`email`

This attribute specifies the email address of the author.

`company`

This attribute specifies the organization to which the author of this design file belongs.

`comment`

This attribute specifies an arbitrary text string used as a comment.

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6.2.3 Example

The following is an example of the `<header>` element in use.

```
<header
    project="JEITA_LPB_SAMPLE_PROJECT"
    design_revision="1.3"
    date="20120331"
    author="yyyyy xxxxx"
    email="xxxx@jeita.jp"
    company="JEITA"
    comment="This is a sample code of LPB format."
/>
```

6.3 The <global> element

6.3.1 General

The `<global>` element defines the unit system, basic shapes, and padstack to be used throughout the R-Format and C-Format files.

```
<global>
             <unit> element
             [<shape> element]…
             [<padstack_def> element]…
</global>
```

The scope of the defined variables is limited to the file in which it is declared. The content of the <global> element consists of one `<unit>` element and one or zero `<shape>` and `<padstack_def>` elements.

6.3.2 The <unit> element

The `<unit>` element defines the unit system to be used in LPB Format file.

```
<unit>
             [<distance> element]
             [<angle> element]
             [<area> element]
             [<time> element]
             [<resistivity> element]
             [<temperature> element]
             [<voltage> element]
             [<power> element]
             [<inductance> element]
             [<frequency> element]
             [<impedance> element]
</unit>
```

The values tell how the numbers found in the LPB Format file shall be interpreted.

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6.3.2.1 Element content

6.3.2.1.1 The <distance> element

The `<distance>` element defines length units in the metric system.

```
<distance unit="length_unit" />
```

The *length_unit* shall be one of the following values:

pm	(picometers)
nm	(nanometers)
um	(micometers)
mm	(millimeters)
m	(meters)
inch	(inches)
mil	mil

6.3.2.1.2 The <angle> element

The `<angle>` element defines a unit system for angles.

```
<angle unit="unit_of_angle" />
```

The *unit_of_angle* shall be either of the following values:

degree
radian

6.3.2.1.3 The <area> element

The `<area>` element defines a unit of area.

```
<area unit="unit_of_area" />
```

The *unit_of_area* shall be one of the following values:

pm2	square picometer
nm2	square nanometer
um2	square micrometer
mm2	square millimeter
m2	square meter

6.3.2.1.4 The <time> element

The `<time>` element defines a unit of time in seconds.

```
<time unit="unit_of_time" />
```

The *unit_of_time* shall be one of the following values:

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`ps`	picosecond
`ns`	nanosecond
`us`	microsecond
`ms`	millisecond
`s`	second

6.3.2.1.5 The <resistivity> element

The `<resistivity>` element defines a unit of resistivity.

```
<resistivity unit="unit_of_resistivity" />
```

The *unit_of_resistivity* shall be one of the following values:

`fohmm`	femtoΩ meter
`nohmm`	nanoΩ meter
`pohmm`	picoΩ meter
`uohmm`	microΩ meter
`mohmm`	milliΩ meter
`ohmm`	Ω meter
`kohmm`	kiloΩ meter
`Mohmm`	megaΩ meter
`Gohmm`	gigaΩ meter

6.3.2.1.6 The <temperature> element

The `<temperature>` element defines a unit system for temperature.

```
<temperature unit="unit_of_temperature" />
```

The *unit_of_temperature* shall be either of the following values:

`C`	Celsius
`K`	Kelvin

6.3.2.1.7 The <voltage> element

The `<voltage>` element defines a unit of voltage.

```
<voltage unit="unit_of_voltage" />
```

The *unit_of_voltage* shall be one of the following values:

`pV`	picovolt
`nV`	nanovolt
`uV`	microvolt
`mV`	millivolt
`V`	volt
`kV`	kilovolt

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6.3.2.1.8 The <power> element

The <power> element defines a unit of power consumption.

```
<power unit="unit_of_power" />
```

The unit_of_power shall be one of the following values:

pW	picowatt
nW	nanowatt
uW	microwatt
mW	milliwatt
W	watt
kW	kilowatt

6.3.2.1.9 The <inductance> element

The <inductance> element defines a unit of inductance.

```
<inductance unit="unit_of_inductance" />
```

The *unit_of_inductance* shall be one of the following values:

fH	femtohenry
pH	picohenry
nH	nanohenry
uH	microhenry
mH	millihenry
H	henry
kH	kilohenry

6.3.2.1.10 The <frequency> element

The <frequency> element defines a unit of frequency.

```
<frequency unit="unit_of_frequency" />
```

The *unit_of_frequency* shall be one of the following values:

uHz	microhertz
mHz	millihertz
Hz	hertz
kHz	kilohertz
MHz	megahertz
GHz	gigahertz

6.3.2.1.11 The <impedance> element

The <impedance> element defines a unit of impedance.

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```
<impedance unit="unit_of_impedance" />
```

The *unit_of_impedance* shall be one of the following values:

fohm	femtoΩ
pohm	picoΩ
nohm	nanoΩ
uohm	microΩ
mohm	milliΩ
Ohm	Ω
kohm	kiloΩ
Mohm	megaΩ

6.3.2.2 Example

The following is an example of the <unit> elements in use.

```
<unit>
  <distance unit="um" />
  <angle unit="degree" />
  <area unit="um2" />
  <time unit="ps" />
  <resistivity unit="ohmm"/>
  <temperature unit="C" />
  <voltage unit="V" />
  <power unit="mW" />
  <inductance unit="nH" />
  <frequency unit="MHz" />
  <impedance unit="ohm" />
</unit>
```

6.3.3 The <shape> element

6.3.3.1 General

The <shape> element defines basic shapes that are referenced by other attributes and elements, such as a <padstack_def> element.

```
<shape>
             [<rectangle> element]…
             [<circle> element]…
             [<polygon> element]…
</shape>
```

The scope of the defined shapes is limited to the file in which it is declared. The content of the <shape> element consists of zero or more <rectangle>, <circle>, and <polygon> element.

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6.3.3.2 Element content

6.3.3.2.1 The <rectangle> element

6.3.3.2.1.1 General

The `<rectangle>` element defines the shape of the rectangle with width, height, and rotation angle.

```
<rectangle
             id="identifier"
             width="width"
             height="height"
             [angle="rotation_angle"]
/>
```

The reference point of the defined rectangle is at the center of the rectangle.

6.3.3.2.1.2 Attribute definitions

The attributes of the `<rectangle>` element are defined as follows.

`id`

This attribute specifies the unique identifier that is used to reference the shape from other attributes and elements.

`width`

This attribute specifies the width of the rectangle. The unit of distance is defined by the `<distance>` element in the `<unit>` element.

`height`

This attribute specifies the height of the rectangle. The unit of distance is defined by the `<distance>` element in the `<unit>` element.

`angle`

This attribute specifies the angle of the counterclockwise rotation with respect to the center of the rectangle. If an angle is not specified, zero is set as the default. The unit of the rotation angle is defined by the `<angle>` element in the `<unit>` element.

6.3.3.2.1.3 Example

The rectangle shape in Figure 12 is represented by the following code:

```
<rectangle id="bfrect10" width="12" height="6"  angle="30" />
```

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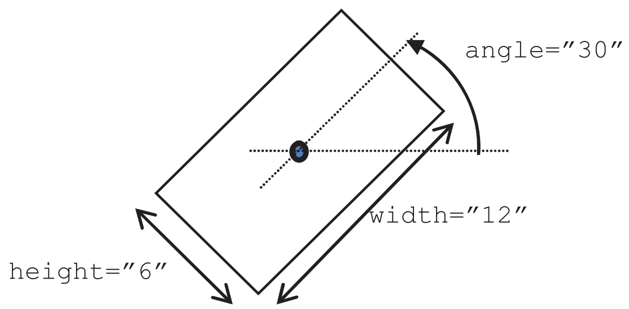

Figure 12—Example of a rectangle shape

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6.3.3.2.2 The <circle> element

6.3.3.2.2.1 General

The `<circle>` element defines the shape of a circle by diameter.

```
<circle
            id="identifier"
            diameter="diameter"
/>
```

The reference point of the circle is at the center.

6.3.3.2.2.2 Attribute definitions

The attributes of the `<circle>` element are defined as follows.

`id`

This attribute specifies the unique identifier that is used to reference the shape from other attributes and elements.

`diameter`

This attribute specifies the diameter of the circle. The unit of distance is defined by the `<distance>` element in the `<unit>` element.

6.3.3.2.2.3 Example

The circle shape in Figure 13 is represented by the following code:

```
<circle id=”viapad12” diameter=”12” />
```

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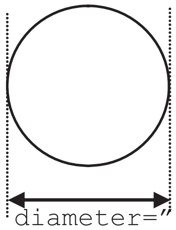

Figure 13—Example of a circle shape

6.3.3.2.3 The <polygon> element

6.3.3.2.3.1 General

The <polygon> element defines the shape of a closed polygon.

```
<polygon
              id="Identifier"
              points="x1, y1, x2, y2, x3, y3, x4, y4 …"
              [angle="rotation_angle"]
/>
```

The reference point of the polygon is set to (0, 0).

6.3.3.2.3.2 Attribute definitions

The attributes of the <polygon> element are defined as follows.

id

This attribute specifies the unique identifier that is used to reference the shape from other attributes and elements.

points

This attribute specifies a sequence of at least four points to generate a closed polygon. The last point and first point shall be same. Points are separated by commas (,), and each point is a pair of XY coordinates separated by a comma (,). The unit of distance is defined by the <distance> element in the <unit> element.

angle

This attribute specifies the angle of the counterclockwise rotation with respect to the reference point of the polygon. If the angle is not specified, zero is set as the default. The unit of the rotation angle is defined by the <angle> element in the <unit> element.

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6.3.3.2.3.3 Example

The polygon shape in Figure 14 is represented by the following code:

```
<polygon id="X1" points="5,3,3,4,-3,2,-1,-3,4,-1,5,3"/>
```

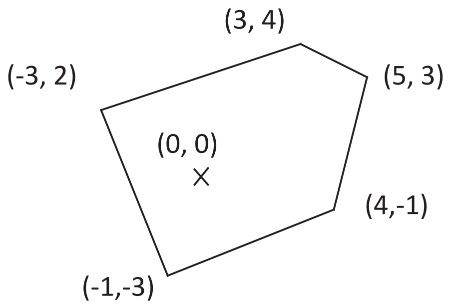

Figure 14—Example of a polygon shape

The polygon shape in Figure 15 is represented by the following code:

```
<polygon id="X2" points="5,3,3,4,-3,2,-1,3,4,-1,5,3" angle="30"/>
```

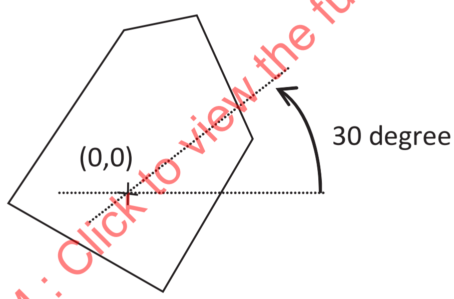

Figure 15—Example of the rotation of a polygon shape

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6.3.3.3 Example

The following is an example of the <shape> elements in use.

```
<shape>
  <rectangle id="R1" width="100" height="10" />
  <circle id="C1" diameter="20" />
  <polygon id="P1" points="-10,-10,10,-10,10,10,-10,10,-10,-10" />
  <circle id="VLLPAD" diameter="500" />
  <circle id="VSLPAD" diameter="400" />
  <circle id="VLSPAD" diameter="700" />
  <circle id="VSAPAD" diameter="600" />
```

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```
  <circle id="SHP.10" diameter="200" />
  <rectangle id="SHP.21" width="7500" height="10900" />
  <polygon id="SQRT" points="10,10,20,10,20,20,20,10,10,10" />
</shape>
```

6.3.4 The <padstack_def> element

6.3.4.1 General

The <padstack_def> element defines padstacks that are referenced by other attributes and elements.

```
<padstack_def
             id="identifier"
>
             {<ref_shape> element}…
</padstack_def>
```

The reference point of the padstack is at local origin (0, 0). The scope of the padstack definitions is limited to the file in which it is declared. The content of the <padstack_def> element consists of one or more <ref_shape> element.

6.3.4.2 Attribute definition

The attribute of the <padstack_def> element is defined as follows.

id

> This attribute specifies the unique identifier that is used to reference the padstack from other attributes and elements.

6.3.4.2.1 The <ref_shape> element

6.3.4.2.1.1 General

The <ref_shape> element references the shape that constructs a padstack.

```
<ref_shape
             shape_id="identifier_of_referenced_shape"
             [type="shape_type"]
             [x="x_coordinate" y="y_coordinate"]
             [angel="rotation_angle"]
             [layer="shape_placed_layer"]
             [pad_layer="pad_placed_layer"]
/>
```

The referenced shape shall be defined at the <shape> element in the same file.

6.3.4.2.1.2 Attribute definitions

The attributes of the <ref_shape> element are defined as follows.

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shape_id

This attribute specifies the identifier of the predefined shape that is defined at the <shape> element. The referenced shape shall be defined at the <shape> element in the same file.

type

This attribute specifies how the shape is used for via structure. Figure 16 shows an example of via structure. The value shall be one of the following:

Antipad	used as a shape of clearance, or antipad
NonConnection	used as a shape of the nonconnection land
Land	used as a shape of the normal land
Drill	used as a shape of the drill; the outside diameter of the via
Hole	used as a shape of the hole; the inside diameter of the via

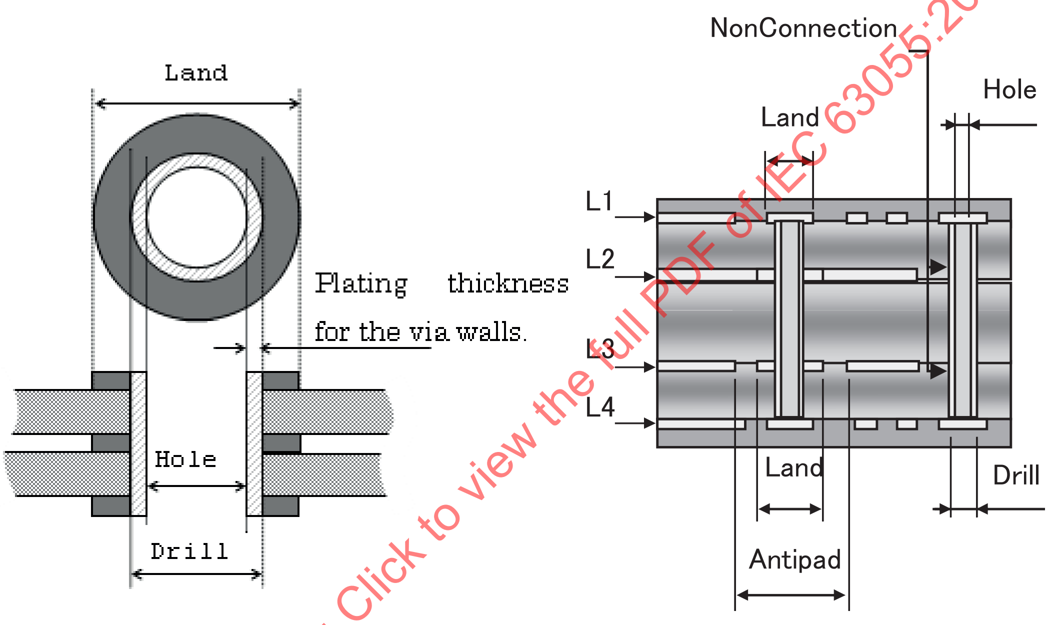

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Figure 16—Example of via structure

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x
y

These attributes specify the location of the reference point of the shape with respect to the local origin. The x and y attributes specify the x-coordinate and y-coordinate, respectively. If these attributes are not specified, zero is set as the default. The unit of the coordinate is defined by the <distance> element in the <unit> element.

angle

This attribute specifies the angle of the counterclockwise rotation with respect to the reference point of the shape. If the angle is not specified, zero is set as the default. The unit of the rotation angle is defined by the <angle> element in the <unit> element.

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`layer`

This attribute specifies the placement layer of the shape. The `layer` attribute is used exclusively by the R-Format.

`pad_layer`

This attribute specifies the placement side of the shape as shown in Figure 17. The `pad_layer` attribute is used exclusively by the C-Format. The value shall be either the following:

`TOP` The shape is placed on the top side.
`BOTTOM` The shape is placed on the bottom side.

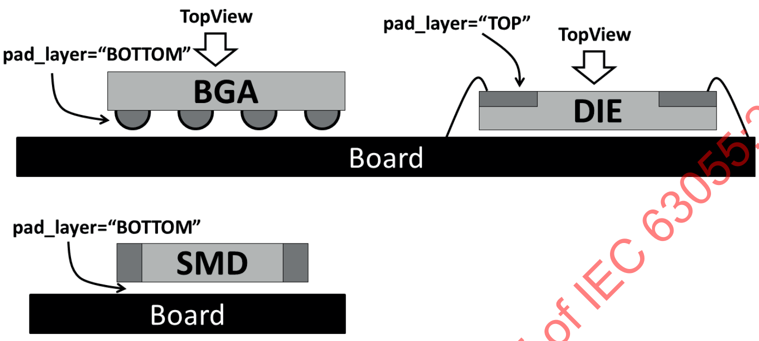

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Figure 17—Explanatory drawing of <pad_layer>

6.3.4.3 Example

The following is an example of the <padstack_def> element in use.

```
<padstack_def>
  <padstack id="smallvia" type="VIA">
     <ref_shape shape_id="VLLPAD" />
     <ref_shape shape_id="VLAPAD"/>
     <ref_shape shape_id="VDRILL" />
     <ref_shape shape_id="VHOLE" />
     <ref_shape shape_id="VLLPAD" />
     <ref_shape shape_id="VLAPAD" />
     <ref_shape shape_id="VDRILL" />
     <ref_shape shape_id="VHOLE"  />
  </padstack>
  <padstack id="ball" type="BALL_PAD">
     <ref_shape shape_id="SHP.10"
                x="0" y="0" angle="0" pad_layer="BOTTOM"
     />
  </padstack>
</padstack_def>XXXX
```

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7. M-Format

7.1 M-Format file structure

The content of the M-Format file consists of one `<header>` element, zero or more `<include>` element, and one or more `<class>` element. The elements shall be specified in the following order:

```
<LPB_MFORMAT>
              <header> element
              [<include> element]…
              {<class> element}…
</LPB_MFORMAT>
```

7.2 The <include> element

7.2.1 General

The `<include>` element specifies other M-Format files to be included.

```
<include
              MFORMAT="name_of_M_format_file"
/>
```

7.2.2 Attribute definition

The attribute of the `<include>` element is defined as follows.

MFORMAT

This attribute specifies the name of the M-Format file to be included. When this attribute does not contain a directory path, it means the M-Format file exists in the current directory. When this attribute contains a relative directory path, it means the M-Format file exists in that relative place from the current directory. Also, this attribute may use an absolute file path from the root directory.

7.2.3 Example

The following is an example of the `<include>` element in use.

```
<include MFORMAT="LPBFMT-PKG.xml" />
<include MFORMAT="ydir/zdir/LPBFMT-PKG2.xml" />
<include MFORMAT="/TOPDIR/xdir/LPBFMT-SOC.xml" />
```

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7.3 The <class> element

7.3.1 General

The <class> element binds the related files that form a functional module, such as an LSI package or printed circuit board.

```
<class
                [comment="comment_text"]
>
                [<CFORMAT> element]
                [<RFORMAT> element]…
                [<GFORMAT> element]…
                [<NFORMAT> element]…
                [<OtherFile> element]…
</class>
```

7.3.2 Attribute definition

The attribute of the <class> element is defined as follows.

comment

This attribute specifies the comment string.

7.3.3 Element content

The <class> element can contain the following elements:

```
<CFORMAT>
<RFORMAT>
<GFORMAT>
<NFORMAT>
<OtherFile>
```

7.3.4 Example

The following is an example of the <class> element in use.

```
<class comment="PWB" >
  <CFORMAT comment="C-Format" file_name="CFMT_TOP.xml"
    design_revision="1.0" " MD5="646da9ae5d90e6b51b0a578badae372f" />
  <RFORMAT comment="R-Format" file_name="RFMT_TOP.xml"
   design_revision="1.0" MD5="6ede01b9fed673b6619cffb5f96e1acf" />
  <GFORMAT comment="G-Format" file_name="GFMT_TOP.xfl"
    MD5="6ede01b9fed672cfa746974210d68e96" />
  <NFORMAT comment="N-Format" file_name="NFMT_TOP.v"
    MD5="ee620bf842fb6646da9ae5d90e6b51b0" />
</class>
```

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7.3.5 The <CFORMAT> element

7.3.5.1 General

The <CFORMAT> element specifies a file of the LPB-component format (C-Format).

```
<CFORMAT
              [comment="comment_text"]
              file_name="name_of_C_format_file"
              design_revision="revision_number"
              [MD5="MD5_checksum"]
/>
```

7.3.5.2 Attribute definitions

The attributes of the <CFORMAT> element are defined as follows.

comment

This attribute specifies a comment string.

file_name

This attribute specifies the name of the C-Format file.

design_revision

This attribute specifies the revision number of the C-Format file.

MD5

This attribute specifies a message digest algorithm 5 (MD5) checksum for the C-Format file.

7.3.5.3 Example

The following is an example of the <CFORMAT> element in use.

```
<CFORMAT comment="C-Format" file_name="CFMT_TOP.xml"
  design_revision="1.0" MD5="5c34a4dd1bb48484e1e93eb5e23b3094" />
```

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7.3.6 The <RFORMAT> element

7.3.6.1 General

The <RFORMAT> element specifies a file of the LPB-rule format (R-Format).

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```
<RFORMAT
              [comment="comment_text"]
              file_name="name_of_R_format_file"
              design_revision="revision_number"
              [MD5="MD5_checksum"]
/>
```

7.3.6.2 Attribute definitions

The attributes of the `<RFORMAT>` element are defined a follows.

`comment`

This attribute specifies a comment string.

`file_name`

This attribute specifies the name of the R-Format file.

`design_revision`

This attribute specifies the revision number of the R-Format file.

`MD5`

This attribute specifies an MD5 checksum for the R-Format file.

7.3.6.3 Example

The following is an example of the `<RFORMAT>` element in use.

```
<RFORMAT comment="R-Format" file_name="RFMT_TOP.xml"
  design_revision="1.0" MD5="4d16098ad69f0a153387d6430a25806a" />
```

7.3.7 The <GFORMAT> element

7.3.7.1 General

The `<GFORMAT>` element specifies a file of the LPB-geometry format (G-Format).

```
<GFORMAT
              [comment="comment_text"]
              file_name="name_of_G_format_file"
              [MD5="MD5_checksum"]
/>
```

7.3.7.2 Attribute definitions

The attributes of the `<RFORMAT>` element are as follows.

`comment`

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This attribute specifies a comment string.

`file_name`

This attribute specifies the name of the G-Format file.

`MD5`

This attribute specifies an MD5 checksum for the G-Format file.

7.3.7.3 Example

The following is an example of the <GFORMAT> element in use.

```
<GFORMAT comment="G-Format" file_name="GFMT_TOP.xfl"
  MD5="b3fed15159e9fbefdf67b603395eaf4c" />
```

7.3.8 The <NFORMAT> element

7.3.8.1 General

The <NFORMAT> element specifies a file of the LPB-netlist format (N-Format).

```
<NFORMAT
             [comment="comment_text"]
             file_name="name_of_N_format_file"
             [MD5="MD5_checksum"]
/>
```

7.3.8.2 Attribute definitions

The attributes of the <NFORMAT> element are defined as follows.

`comment`

This attribute specifies a comment string.

`file_name`

This attribute specifies the name of the N-Format file.

`MD5`

This attribute specifies an MD5 checksum for the N-Format file.

7.3.8.3 Example

The following is an example of the <NFORMAT> element in use.

```
<NFORMAT comment="N-Format" file_name="NFMT_TOP.v"
  MD5="343490687786f1420958e9aed2f2895b" />
```

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7.3.9 The <OtherFile> element

7.3.9.1 General

The `<OtherFile>` element specifies the names of user-defined files.

```
<OtherFile
             [comment="comment_text"]
             file_name="name_of_format_file"
             [MD5="MD5_checksum"]
/>
```

7.3.9.2 Attribute definitions

The attributes of the `<OtherFile>` element are defined as follows.

`comment`

This attribute specifies a comment string.

`file_name`

This attribute specifies the name of a user-defined file.

`MD5`

This attribute specifies an MD5 checksum for the user-defined file.

7.3.9.3 Example

The following is an example of the `<OtherFile>` element in use.

```
<OtherFile comment="Power Model" file_name="DDRPowerModel.sp"
MD5="7ca273b0993527d8df5deed246b8fbff" />
```

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8. C-Format

8.1 C-Format file structure

The content of the C-Format file consists of one `<header>` and `<global>` element, one or more `<model>` elements, and one or zero `<component>` element. These elements shall be specified in the following order:

```
<LPB_CFORMAT>
             <header> element
             <global> element
             {<module> element}…
             [<component> element]
</LPB_CFORMAT>
```

8.2 The <module> element

8.2.1 General

The module is the basic design unit of items such as a semiconductor chip or LSI package. The <module> element encapsulates the geometry information, design constraints, I/O interface, and electrical model of a module.

```
<module
             name="name_of_module"
             type="module_type"
             [shape_id="identifier_of_referenced_shape"]
             [x="x_coordinate"   y="y_coordinate"]
             [angle="angle"]
             [thickness="thickness"]
>
             {<socket> element}…
             [<specification> element]
             {<reference> element}…
</module>
```

The content of the <module> element consists of zero or more <socket> and <reference> elements and one or zero <specification> element.

The <socket> element defines the I/O ports and design constraints.

The <specification> element defines the specifications for the module itself, such as power consumption.

The <reference> element associates the port defined in the <socket> element with electrical node or physical data that are defined in other files. For example, the <reference> element can provide the position for the I/O node of IBIS that does not have a physical information.

8.2.2 Attribute definitions

The attributes of the <module> element are as follows:

name

This attribute specifies the module name that is used to reference the module from other attributes and elements. The module name shall be unique in the same C-Format file.

type

This attribute specifies the module type. The value shall be one of the following:

LSI	semiconductor integrated circuit
PKG	package
PWB	printed wiring board or printed circuit board.
OTHER	other type

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shape_id

This attribute specifies the identifier of the predefined shape to define the boundary shape of the module. The specified shape shall be defined at the <shape> element in the same file.

x
y

These attributes specify the location of the reference point of the shape with respect to the local origin. The x and y attribute specify the x-coordinate and y-coordinate, respectively. The module is placed at the specified point (see Figure 18). If these attributes are not specified, zero is set as the default. The unit of the coordinates is defined by the <distance> element in the <unit> element.

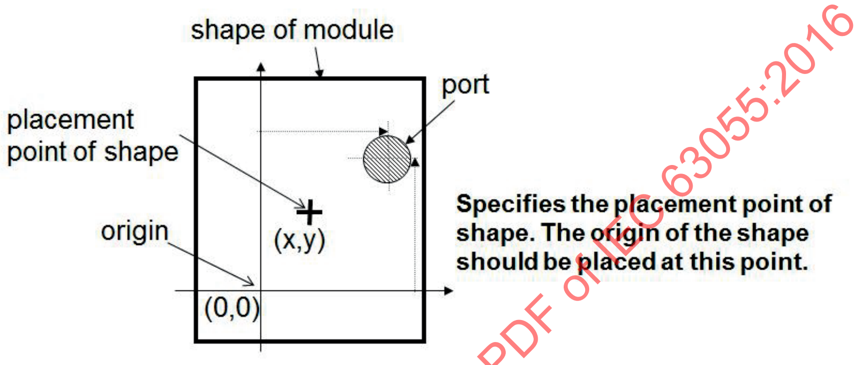

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Figure 18—Example of the shape of the module and its placement

angle

This attribute specifies the angle of the counterclockwise rotation with respect to the reference point of the shape as shown in Figure 19. If the angle is not specified, zero is set as the default. The unit of the rotation angle is defined by the <angle> element in the <unit> element.

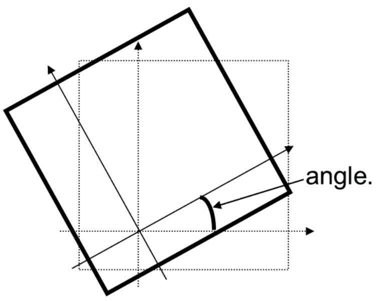

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Figure 19—Explanatory drawing of the rotation of a module

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`thickness`

This attribute specifies the thickness module without pin or solder-ball, as shown in Figure 20. If the thickness is not specified, zero is set as the default. The unit of the coordinate is defined by the `<distance>` element in the `<unit>` element.

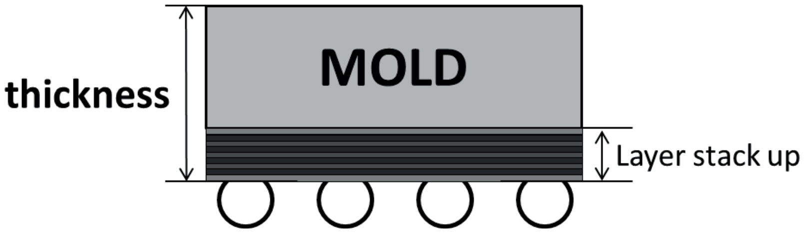

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Figure 20—Explanatory drawing of the `thickness` attribute of the module

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8.2.3 Example

The following is an example of the `<module>` element in use.

```
<global>
    <shape>
        <rectangle id="PFGBABODY"   width="1200"  height="1200" />
        <circle id="B500" circle="500" />
    </shape>
    <padstack_def>
         <padstack id="BGABALL" type="BALLPAD">
             <ref_shape shape_id="B500" x="0" y="0" />
         </padstack>
    </padstack_def>
</global>
<module  name="BGA" type="PKG"
              shape_id="PFBGABODY" x="0" y="0" thickness="540">
   <socket  name="BGAIO" >
      <default>
          <port_shape padstack_id="BGABALL" />
      </default>
      <port id="A1" x="-1100" y="-1100" />
      <port id="A2" x="-1000" y="-1100" />
   </socket>
</module>
```

8.2.4 The <socket> element

8.2.4.1 General

The `<socket>` element defines the I/O ports and design constraints.

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```
<socket
             name="socket_name"
>
             [ <default> element ]
             { <port> element }…
             [ <portgroup> element ]…
             [ <powerdomain_group> element ]…
             [ <swappable_port> element ]…
             [ <swappable_group> element ]…
             [ <frequency> element ]…
             [ <constraint> element ]…
</socket>
```

The port definition is not only logical information but also geometrical information. The logical information includes the signal direction, name, and type. The geometrical information includes the shape and location of the port, like a footprint. The design constraints provide constraints to route the signal connecting the module.

The <socket> element can contain the following elements:

```
<default>
<port>
<portgroup>
<powerdomain_group>
<swappable_port>
<swappable_group>
<frequency>
<constraint>
```

The <port> element defines the I/O ports, and the <default> element defines the default shape for ports. Each port can have a different shape, but if all ports have the same shape, the <default> element can be used.

The <portgroup> element defines sets of ports that are referred to by other elements in the same file.

The <powerdomain_group> element defines the power domain of the signals that move in and out from the port of the module. The <swappable_port> and <swappable_group> elements define sets of swappable ports to each other, like double data rate 3 synchronous dynamic random access memory (DDR3 SDRAM) data bus bytes. The <frequency> element defines the operating frequency for signals that move in and out from the port of the module. The <constraint> element defines the design constraints, such as limitation of skew.

Figure 21 shows examples of sockets. In the case of a BGA package, the socket is a set of solder balls. A <module> element may have multiple <socket> elements. Diagram (b) in Figure 21 shows an example of a printed wiring board. In this example, the one card edge and the two connectors are defined as the socket.

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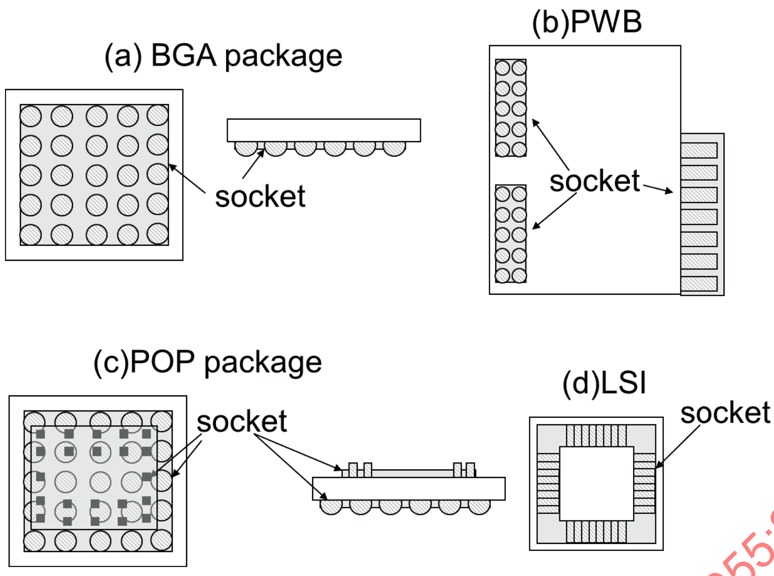

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Figure 21 —Explanatory drawing of the structure of sockets and modules

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8.2.4.2 Attribute definition

The attribute of the `<socket>` element is defined as follows.

`name`

This attribute specifies the socket name that is used to reference the socket from other attributes and elements. The socket name shall be unique in the same C-Format file.

8.2.4.3 Element content

The `<socket>` element can contain the following elements:

```
<default>
<port>
<portgroup>
<powerdomain_group>
<swappable_port>
<swappable_group>
<frequency>
<constraint>
```

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8.2.4.4 The <default> element

8.2.4.4.1 General

The <default> element defines the default shapes for the port that are used when the shape is not defined in the <port> element.

```
<default>
              [<port_shape> element]
              [<ball_shape> element]
</default>
```

The content of the <default> element consists of zero or one <port_shape> and <ball_shape> elements, which define the pad and solder ball shape, respectively.

8.2.4.4.2 The <port_shape> element

8.2.4.4.2.1 General

The <port shape> element defines the default pad shape for the I/O port.

```
<port_shape padstack_id="identifier_of_referenced_padstack" />
```

The default is used when the pad shape is not defined in the <port> element.

8.2.4.4.2.2 Attribute definition

The attribute of the <port_shape> element is defined as follows.

padstack_id

This attribute specifies the identifier of the predefined padstack that is used to define the default pad shape. The referenced padstack shall be defined at the <padstack_def> element in the same file.

8.2.4.4.2.3 Example

The following is an example of the <port_shape> element in use.

```
<global>
  <shape>
    <circle id="circ_3" diameter="1500" />
    <circle id="circ_4" diameter="750" />
  </shape>
  <padstack_def>
    <padstack id="PAD.4" >
      <ref_shape shape_id="circ_3" type="Land"
              x="0" y="0" pad_layer="TOP" />
      <ref_shape shape_id="circ_4" type="Hole"
              x="0" y="0" pad_layer="TOP" />
      <ref_shape shape_id="circ_3" type="Land"
              x="0" y="0" pad_layer="BOTTOM" />
```

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```
    <ref_shape shape_id="circ_4" type="Hole"
            x="0" y="0" pad_layer="BOTTOM" />
   </padstack>
  </padstack_def>
</global>
<module name="LPB_2012_SAMPLE" type="PWB" shape_id="SHAPE.1"
             x="0" y="0" angle="0" >
  <socket  name="SMA_X1" >
   <default>
    <port_shape padstack_id="PAD.4" />
   </default>
   <port id="1" x="1570.7" y="32293.2" />
   <port id="2" x="-429.3" y="34293.2" />
   <port id="3" x="-429.3" y="30293.2" />
   <port id="4" x="3570.7" y="30293.2"/>
   <port id="5" x="3570.7" y="34293.2"/>
  </socket>
</module>
```

8.2.4.4.3 The <ball shape> element

8.2.4.4.3.1 General

The <ball_shape> element defines the default solder ball shape for the I/O port of the BGA package.

```
<ball_shape ball_name="name_of_referenced_ball" />
```

The default is used when the solder ball shape is not defined in the <port> element.

8.2.4.4.3.2 Attribute definition

The attribute of the <ball_shape> element is defined as follows.

ball_name

> This attribute specifies the name of the ball that is used to define the default shape of the solder ball. The referenced ball is defined at the <ball_def> element in the R-Format file.

8.2.4.4.3.3 Example

The following is an example of the <port_shape> element in use.

```
<ball_shape ball_name="BGA_BALL" />
```

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8.2.4.5 The <port> element

8.2.4.5.1 General

The <port> element defines the logical and geometry information for a port of the module.

```
<port
       [id="identifier"
              [padstack_id="identifier_of_referenced_padstack"]
              [ball_name="name_of_reference_ball"]
              [x="x_coordinate" y="y_coordinate"]
              [angle="angle"]
       ]
       [name="port_name"
              [direction="signal_direction"]
              [type="signal_type"]
       ]
>
              [<impedance> element]
              [<delay> element]
</port>
```

The logical information is the port name, signal direction, and signal type. These are defined by the name, direction, and type attributes, respectively. The geometry information is the port identifier, port shape, and location. These are defined by the padstack_id, ball_name, x, y, and angle attributes. The <port> element can have both logical and geometry information or it can have only one type of information.

The content of the <port> element consists of zero or one <impedance> and <delay> elements. The actual impedance and delay are defined by these elements.

8.2.4.5.2 Attribute definitions

The attributes of the <port> element are defined as follows.

id

This attribute specifies the unique identifier that is used to reference the port from other attributes and elements. The identifier shall be unique in the <socket> element. Normally, the id follows the Joint Electron Device Engineering Council's (JEDEC's) naming convention. In the case of a BGA package, the id might be A1, A2, A3, etc.

padstack_id

This attribute specifies the identifier of a predefined padstack to define the shape of the port. The referenced padstack shall be defined at the <padstack_def> element in the same file. If the padstack_id is not specified, the default shape that is defined in the <default> element is used.

ball_name

This attribute is used for BGA packages. Specify the name of the ball to define the shape of the solder-ball. The referenced ball is defined at the <ball_def> element in the R-Format file. If the ball_name is not specified, the default shape that is defined in the <default> element in the same <socket> element is used.

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x
y

These attributes specify the location of the reference point of the referenced padstack with respect to the local origin of the module. The x and y attributes specify the x-coordinate and y-coordinate, respectively. The unit of the coordinates is defined by the <distance> element in the <unit> element.

angle

This attribute specifies the angle of the counterclockwise rotation with respect to the local origin of the module. If the angle is not specified, zero is set as the default. The unit of the rotation angle is defined by the <angle> element in the <unit> element.

name

This attribute specifies the name of a port. Normally, the port name is the same as the signal that inputs/outputs from the port. The same name can be used for different ports. For example, the ports that connect to the same ground plane can have the same port name.

direction

This attribute specifies the signal direction for a port as shown in Figure 22. The value shall be one of the following:

in port that accepts signals coming in to the module
out port that drives signals out of the module
inout port that can accept signals going either in or out of the module; power and ground types of port shall be inout.

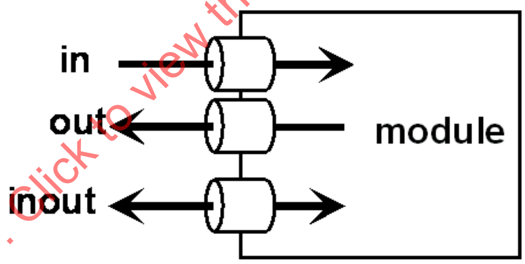

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Figure 22 —Explanatory drawing of the relation of in/out/inout ports and signal direction

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type

This attribute specifies the port type for a port. The value shall be one of the following.

power port is used for power distribution network.
ground port is used for ground distribution network.
signal port is used for signal net.
floating port shall not be connected to any net
dontcare port does not have any logical meanings, such as thermal ball
through port that goes completely across the module, namely, feed-through

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The signal direction of `floating`, `dontcare`, and `through` ports is ignored.

8.2.4.5.3 Element content

The `<port>` element can contain the following elements:

```
<impedance>
<delay>
```

8.2.4.5.4 Example

The following is an example of the `<port>` element in use.

```
<port id="A1" x="-12500" y="12500" direction="input">
    <impedance typ="50"/>
    <delay typ="100"/>
</port>

<port id="A2" x="-11500" y="12500" direction="output">
    <impedance typ="50"/>
    <delay typ="100"/>
</port>
```

8.2.4.5.5 The <impedance> element

8.2.4.5.5.1 General

The `<impedance>` elements define the actual I/O impedance for the port.

```
<impedance typ="port_impedance" />
```

8.2.4.5.5.2 Attribute definition

The attribute of the `<impedance>` element is as follows.

`typ`

This attribute specifies an actual load impedance of the port. The unit of impedance is defined by the `<impedance>` element in the `<unit>` element.

8.2.4.5.6 The <delay> element

8.2.4.5.6.1 General

The `<delay>` element defines the actual backward delay and the forward delay, which are the delays from the input port to the internal logic and vice versa.

```
<delay typ="port_delay" />
```

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8.2.4.5.6.2 Attribute definition

The attribute of the <delay> element is defined as follows.

typ

This attribute specifies an actual delay of the port. The unit of delay is defined by the <time> element in the <unit> element.

8.2.4.6 The <portgroup> element

8.2.4.6.1 General

The <portgroup> element defines groups of ports that are referenced by other elements in the same file.

```
<portgroup
              name="port_group_name"
>
              [<mousjoin/>]
              [<ref_port> element]…
              [<ref_portgroup> element]…
</portgroup>
```

A port can belong to multiple groups if necessary. The groups can nest into other groups. It is possible to create a new port group by collecting multiple port groups.

8.2.4.6.2 Attribute definition

The attribute of the <portgroup> element is defined as follows.

name

This attribute specifies the name of the port group that is used to reference the group from other attributes and elements. The group name shall be unique in the <socket> element.

8.2.4.6.3 Element content

The <portgroup> element can contain the following elements:

<mustjoin>
<ref_port>
<ref_portgroup>

8.2.4.6.4 Example

The following is an example of the <portgroup> element in use.

```
<portgroup name="ADD">
      <ref_port name="AD0" />
      <ref_port name="AD1" />
      <ref_port name="AD2" />
      <ref_port name="AD3" />
```

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```
</portgroup>

<portgroup name="DIGITAL_GND">
    <mustjoin/>
    <ref_port name="CORE_GND" />
    <ref_port name="IO_GND" />
</portgroup>

<portgroup name="ANALOG_GND">
    <mustjoin/>
    <ref_port id="A1" />
    <ref_port id="A2" />
</portgroup>

<portgroup name="GND">
    <ref_portgroup name="DIGITAL_GND" />
    <ref_portgroup name="ALALOG_GND" />
</portgroup/>
```

8.2.4.6.5 The <mustjoin> element

If `<mustjoin/>` is contained in the `<port group>` element, the ports in the group shall be connected together.

```
<mustjoin/>
```

8.2.4.6.6 The <ref_port> element

8.2.4.6.6.1 General

The `<ref_port>` element refers to the ports that make up the group.

```
<ref_port
             { id="identifier_of_referenced_port" |
              name="name_of_referenced_port"  }
/>
```

The port shall be specified with either the name (`name`) or the identifier (`id`). The referred port shall be defined in the same `<socket>` element.

8.2.4.6.6.2 Attribute definitions

The attributes of the `<ref_port>` element are defined as follows.

`id`

> This attribute specifies the identifiers of the predefined ports that make up the group. The specified port shall be defined at the `<port>` element in the same `<socket>` element. The `id` attribute shall not be used with the `name` attribute.

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name

This attribute specifies the names of the predefined ports that make up the group. The specified port shall be defined at the <port> element in the same <socket > element. The name attribute shall not be used with the id attribute. If multiple same-name ports exist, these ports belong to the same group.

8.2.4.6.7 The <ref_portgroup> element

8.2.4.6.7.1 General

A port group can nest into another port group. The <ref_portgroup> element refers to the other port group.

```
<ref_portgroup
              name="name_of_referenced_port_group"
/>
```

The referenced port group shall be defined in the same <socket> element.

8.2.4.6.7.2 Attribute definition

The attribute of the <ref_portgroup> element is defined as follows.

name

This attribute specifies the name of the predefined port group that makes up the nested group. The specified port group shall be defined in the same <socket> element.

8.2.4.7 The <powerdomain_group> element

8.2.4.7.1 General

The <powerdomain_group> element defines the power domain of the signals that move in and out from the port of the module.

```
<powerdomain_group
              { port_name="name_of_referenced_port" |
              port_id="identifier_of_referenced_port" |
              group_name="name_of_referenced_port_group" }
              [min="minimum_voltage"]
              typ="typical_voltage"
              [max="maximum_voltage"]
>
              [<ref_portgroup> element]
              [<ref_port> element]
</powerdomain_group>
```

For example, in the case of analog-digital mixed design, this element specifies the analog power/ground and analog signals that make up the power domain in order to distinguish them from the digital. The port shall be specified with either the port name (port_name), port identifier (port_id), or port group name (group_name). The referenced port or port group shall be defined in the same <socket> element.

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8.2.4.7.2 Attribute definitions

The attributes for the <powerdomain_group> element are defined as follows.

port_name

This attribute specifies the name of the power or ground port that defines the voltage level of the power domain. The referenced power or ground port shall be defined at the <port> element in the same <socket> element, and the port type shall be power or ground. The port_name attribute shall not be used with the port_id and group_name attributes.

port_id

This attribute specifies the identifier of the power or ground port that defines the voltage level of the power domain. The referenced power or ground port shall be defined at the <port> element in the same <socket> element, and the port type shall be power or ground. The port_id attribute shall not be used with the port_name and group_name attributes.

group_name

This attribute specifies the name of the port group that defines the voltage level of the power domain. The specified port group shall be defined at the <portgroup> element in the same <socket> element. The type of the ports that belong to the group shall be power or ground. The group_name attribute shall not be used with the port_name and port_id attributes.

typ

This attribute specifies the typical voltage level. The voltage perturbation is specified by min and max attributes. The unit of voltage is defined by the <voltage> element in the <unit> element.

min
max

These attributes specify the voltage perturbation level. The max and min attributes are the maximum and minimum voltage, respectively. The unit of voltage is defined by the <voltage> element in the <unit> element.

8.2.4.7.3 Element content

The <powerdomain_group> element can contain the following elements:

<ref_portgroup>
<ref_port>

8.2.4.7.4 Example

The following is an example of the <powerdomain_group> element in use.

```
<portgroup name="DCDC_25V">
   <ref_port name="SWOUT1" />
   <ref_port name="SWOUT2" />
</portgroup>
<portgroup name="DCDC_CTRL">
   <ref_port name="FB" />
   <ref_port name="LDO" />
```

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```
</portgroup>
<portgroup name="DDR_DIG" />
  <ref_port name="PL1" />
  <ref_port name="PL2" />
  <ref_port name="PL3" />
  <ref_port name="PL4" />
</portgroup>

<powerdomain_group  port_name="DCDC_PGND"  typ="2.5">
     <ref_portgroup  name="DCDC_25V" />
     <ref_portgroup  name="DCDC_CTRL" />
     <ref_portgroup name="DDR_DIG" />
</powerdomain_group>
<powerdomain_group port_name="D_GND" typ="0" >
     <ref_portgroup  name="DCDC_25V" />
     <ref_portgroup  name="DCDC_CTRL" />
     <ref_portgroup name="DDR_DIG" />
</powerdomain_group>
```

8.2.4.7.5 The <ref_portgroup> element

8.2.4.7.5.1 General

The <ref_portgroup> element refers to the port group that makes up the power domain.

```
<ref_portgroup
             name="name_of_referenced_port_group"
/>
```

The referenced port group shall be defined in the same <socket> element.

8.2.4.7.5.2 Attribute definition

The attribute of the <ref_portgroup> element is defined as follows.

name

This attribute specifies the name of the predefined port group that makes up a power domain. The ports that are included in the same group belong to the same power domain. The specified port group shall be defined in the same <socket> element.

8.2.4.7.6 The <ref_port> element

8.2.4.7.6.1 General

The <ref_port> element refers to the port that makes up the power domain.

```
<ref_port
             { id="identifier_of_referenced_port" |
               name="name_of_referenced_port" }
/>
```

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The port shall be specified with either the name (name) or the identifier (id). The referenced port shall be defined in the same <socket> element.

8.2.4.7.6.2 Attribute definitions

The attributes of the <ref_port> element are defined as follows.

id

This attribute specifies the identifiers of the predefined ports that make up a power domain. The specified port shall be defined at the <port> element in the same <socket> element. The id attribute shall not be used with the name attribute.

name

This attribute specifies the name of the predefined ports that make up a power domain. The specified port shall be defined at the <port> element in the same <socket> element. The name attribute shall not be used with the id attribute. If multiple same-name ports exist, these ports belong to the same power domain.

8.2.4.8 The <swappable_port> element

8.2.4.8.1 General

The <swappable_port> element defines sets of swappable ports, such as DDR3 data bus bytes.

```
<swappable_port>
             <ref_port> element
             {<ref_port> element}…
</swappable_port>
```

The nets that are connected to the swappable <swappable_port> ports can replace each other in the connection. For example, if the swappable CK_N and CK_P shown in Figure 23 are connected to n1 and n2, respectively, you can swap the connection of CK_N and CL_P.

8.2.4.8.2 Element content

The <swappable_port> element contains the following element:

<ref_port>

8.2.4.8.3 Example

The swappable ports shown in Figure 23 are represented by the following code:

```
<swappable_port>
   <ref_port name="CK_N" />
   <ref_port name="CK_P" />
</swappable_port>
```

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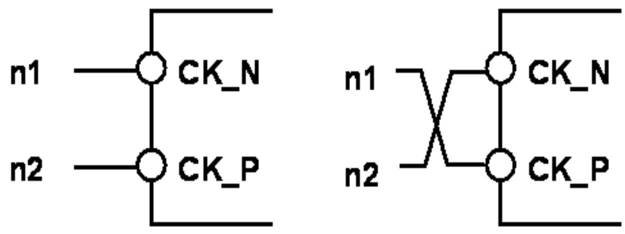

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Figure 23 —Example of swappable ports

8.2.4.8.4 The <ref_port> element

8.2.4.8.4.1 General

The <ref_port> element refers to the ports that make up the swappable port group.

```
<ref_port
            { id="identifier_of_referenced_port" |
             name="name_of_reference_port" }
/>
```

The port shall be specified with either the name (name) or the identifier (id) attribute. The referenced port group shall be defined in the same <socket> element.

8.2.4.8.4.2 Attribute definitions

The attributes of the <ref_port> element are as follows.

id

This attribute specifies the identifier of the predefined ports that make up a set of swappable ports. The specified ports shall be defined at the <port> element in the same <socket> element. The id attribute shall not be used with the name attribute.

name

This attribute specifies the names of the predefined ports that make up a set of swappable ports. The specified ports shall be defined at the <port> element in the same <socket> element. The name attribute shall not be used with the id attribute.

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8.2.4.9 The <swappable_group> element

8.2.4.9.1 General

The <swappable_group> element defines sets of swappable port groups.

```
<swappable_group>
             <ref_portgroup> element
             {<ref_portgroup> element}…
</swappable_group>
```

The port groups in the same <swappable_group> are swappable by a group unit (see Figure 24 and Figure 25).

8.2.4.9.2 Element content

The <swappable_group> element contains the following elements:

<ref_portgroup>

8.2.4.9.3 Example

The swappable group shown in Figure 24 is represented by the following code:

```
<portgroup name="R_CHANNEL">
   <ref_port name="RAD1" />
   <ref_port name="RAD2" />
   <ref_port name="RAD3" />
</portgroup>
<portgroup name="L_CHANNEL" />
   <ref_port name="LAD1" />
   <ref_port name="LAD2" />
   <ref_port name="LAD3" />
</portgroup>

<swappable_group>
   <ref_portgroup name="R_CHANNEL" />
   <ref_portgroup name="L_CHANNEL" />
</swappable_group>
```

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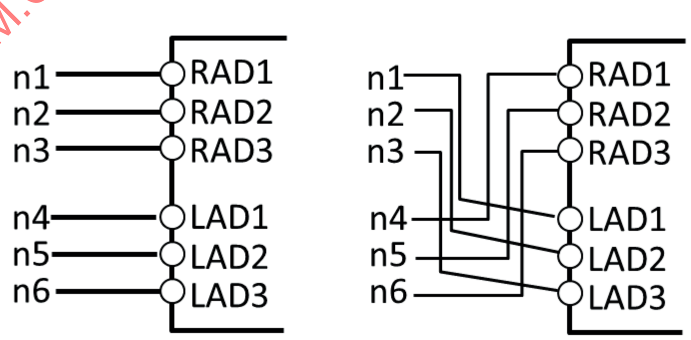

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Figure 24—Example of a swappable group

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The swappable group shown in Figure 25 is represented by the following code:

```
<portgroup name="RCHA_1">
   <ref_port name="RAD1" />
   <ref_port name="RAD2" />
</portgroup>
<portgroup name="RCHA_2">
   <ref_port name="RAD3" />
   <ref_port name="RAD3" />
</portgroup>
<portgroup name="R_CHANEL" />
   <ref_portgroup="RCHA_1" />
   <ref_portgroup="RCHA_2" />
</portgroup>
<portgroup name="L_CHANNEL" />
   <ref_port name="LAD1" />
   <ref_port name="LAD2" />
   <ref_port name="LAD3" />
   <ref_port name="LAD4" />
</portgroup>
<swappable_group>
   <ref_portgroup name="R_CHANNEL" />
   <ref_portgroup name="L_CHANNEL" />
</swappable_group>
```

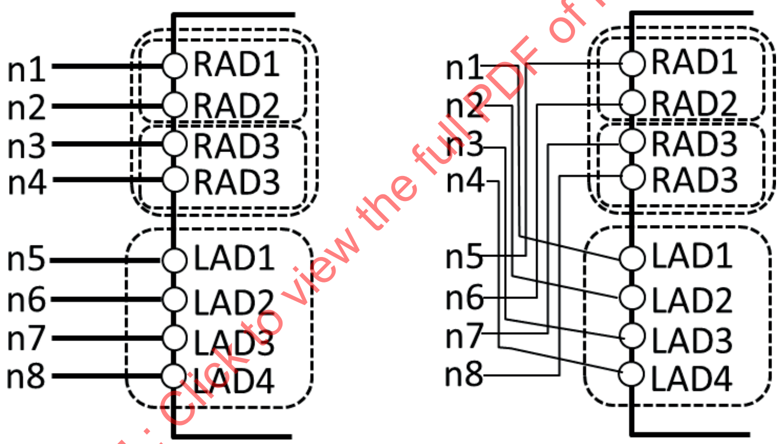

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Figure 25—Example of a swappable group

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8.2.4.9.4 The <ref_portgroup> element

8.2.4.9.4.1 General

The `<ref_portgroup>` element refers to two or more port groups.

```
<ref_portgroup
              name="group_name_of_reference_port"
/>
```

The ports belonging to the referenced groups can be swapped. For example, if the following two port groups, AGRP and BGRP, are swappable groups, ports A0 and B0, A1 and B1, and A2 and B2 are swappable, respectively.

```
<portgroup name="AGRP">
   <ref_port name="A0" />
   <ref_port name="A1" />
   <ref_port name="A2" />
</portgroup>

<portgroup name="BGRP">
   <ref_port name="B0" />
   <ref_port name="B1" />
   <ref_port name="B2" />
</portgroup>
```

8.2.4.9.4.2 Attribute definition

The attribute for the <ref_portgroup> element is defined as follows.

name

This attribute specifies the name of the predefined port groups that make up a set of swappable ports. The specified port groups shall be defined in the same <socket> element.

8.2.4.10 The <frequency> element

8.2.4.10.1 General

The <frequency> element defines the minimum, typical, and maximum operating frequencies for signals that move in and out of the port of the module.

```
<frequency
             { port_name="name_of_reference_port" |
              port_id="identifier_of_reference_port" |
              group_name="identifier_of_reference_port_group" }
             min="minimum_frequency"
             [typ="typical_frequency"]
             max="maximum_frequency"
/>
```

The port shall be specified with either the port name (port_name), port identifier (port_id), or group name (group_name).

8.2.4.10.2 Attribute definitions

The attributes of the <frequency> element are defined as follows.

port_name

This attribute specifies the name of a predefined port for inputting and outputting a signal that defines the operating frequency. The specified port shall be defined at the <port> element in the same <socket> element. The port_name attribute shall not be used with the port_id and group_name attributes.

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port_id

This attribute specifies the identifier of a predefined port for inputting and outputting a signal that defines the operating frequency. The specified port shall be defined at the <port> element in the same <socket> element. The port_id attribute shall not be used with the port_name and group_name attributes.

group_name

This attribute specifies the name of a group that includes ports for inputting and outputting a signal that defines the operating frequency. The ports included in the specified group are operating at the same frequency. The specified port group shall be defined at the <portgroup> element in the same <socket> element. The group_name attribute shall not be used with the port_name and port_id attributes.

typ

This attribute specifies the typical frequency. The frequency perturbation is specified by the min and max attributes. The unit of frequency is defined by the <frequency> element in the <unit> element.

min
max

These attribute specifies the frequency perturbation. The max and min attributes are the maximum and minimum frequencies, respectively. The unit of frequency is defined by the <frequency> element in the <unit> element.

8.2.4.10.3 Example

The following is an example of the <frequency> element in use.

```
<frequency port_name="FKBCLK" max="55" />
```

8.2.4.11 The <constraint> element

8.2.4.11.1 General

The <constraint> element defines the design constraints, such as limitation of skew.

```
<constraint>
             [<impedance> element]
             [<delay> element]
             [<skew> element]
             [<guard_shield> element]
</constraint>
```

The <constraint> element consists one or more <impedance>, <delay>, and <skew> elements.

8.2.4.11.2 Element content

The <constraint> element can contain the following elements:

<impedance>

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```
<delay>
<skew>
<guard_shield>
```

8.2.4.11.3 The <impedance> element

8.2.4.11.3.1 General

The `<impedance>` element defines the minimum, typical, and maximum characteristic impedances for the port that requests impedance matching.

```
<impedance
             { port_name="name_of_reference_port" |
               port_id="identifier_of_referenced_port" |
               group_name="name_of_reference_port_group"   }
             [type="impedance_type"]
             [min="minimum_impedance"]
             typ="typical_impedance"
             [max="maximum_impedance"]
/>
```

The port shall be specified with either the port name (`port_name`), port identifier (`port_id`), or group name (`group_name`) attribute.

8.2.4.11.3.2 Attribute definitions

The attributes for the `<impedance>` element are defined as follows.

`port_name`

This attribute specifies the name of a predefined port for inputting and outputting a signal that requests impedance matching. The specified port shall be defined at the `<port>` element in the same `<socket>` element. The `port_name` attribute shall not be used with the `port_id` and `group_name` attributes.

`port_id`

This attribute specifies the identifier of a predefined port for inputting and outputting a signal that requests impedance matching. The specified port shall be defined at the `<port>` element in the same `<socket>` element. The `port_id` attribute shall not be used with the `port_name` and `group_name` attributes.

`group_name`

This attribute specifies the name of a group that includes ports for inputting and outputting a signal that requests impedance matching. The specified port group shall be defined at the `<portgroup>` element in the same `<socket>` element. The `group_name` attribute shall not be used with the `port_name` and `port_id` attributes.

`type`

This attribute specifies the type of the characteristic impedance. The value shall be one of the following:

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`single`	single-ended signal
`differential`	differential mode impedance
`common`	common mode impedance

If the `type` attribute is not defined, `single` is set as the default.

`typ`

This attribute specifies the typical impedance value. The impedance perturbation is specified by the `min` and `max` attributes. The unit of impedance is defined by the `<impedance>` element in the `<unit>` element.

`min`
`max`

These attributes specify the impedance perturbation. The `max` and `min` attributes are the maximum and minimum impedance values, respectively. The unit of impedance is defined by the `<impedance>` element in the `<unit>` element.

8.2.4.11.3.3 Example

The following is an example of the `<impedance>` element in use.

```
<portgroup name="CK">
   <ref_port port_name="CK_N" />
   <ref_port port_name="CK_P" />
</portgroup>
<constraint>
 <impedance port_name="DQ1" type="single" min="45" typ="50" max="55" />
 <impedance port_id="A1" type="single" typ="50" />
 <impedance group_name="CK" type="differential" typ="100" />
</constraint>
```

8.2.4.11.4 The <delay> element

8.2.4.11.4.1 General

The `<delay>` element defines the minimum, typical, and maximum delay value for the port that requests a timing constraint.

```
<delay
             { port_name="name_of_referenced_port" |
              port_id="identifier_of_referenced_port" |
              group_name="name_of_referenced_port_group"}
             [min="minimum_delay"]
             typ="typical_delay"
             [max="maximum_delay"]
/>
```

The port shall be specified with the port name (`port_name`), port identifier (`port_id`), or group name (`group_name`) attribute.

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8.2.4.11.4.2 Attribute definitions

The attributes of the <delay> element are defined as follows.

port_name

This attribute specifies the name of a predefined port for inputting and outputting a signal that requests a timing constraint. The specified port shall be defined at the <port> element in the same <socket> element. The port_name attribute shall not be used with the port_id and group_name attributes.

port_id

This attribute specifies the identifier of a predefined port for inputting and outputting a signal that requests a timing constraint. The specified port shall be defined at the <port> element in the same <socket> element. The port_id attribute shall not be used with the port_name and group_name attributes.

group_name

This attribute specifies the name of a group that includes ports for inputting and outputting a signal that requests a timing constraint. The specified port group shall be defined at the <portgroup> element in the same <socket> element. The group_name attribute shall not be used with the port_name and port_id attributes.

typ

This attribute specifies the typical delay value. The delay time perturbation is specified by the min and max attributes. The unit of delay is defined by the <time> element in the <unit> element.

min
max

These attributes specify the delay time perturbation. The max and min attributes are the maximum and minimum delay values, respectively. The unit of delay is defined by the <time> element in the <unit> element.

8.2.4.11.4.3 Example

The following is an example of the <delay> element in use.

```
<portgroup name="BUS">
   <ref_port port_name="SIG1" />
   <ref_port port_name="SIG2" />
   <ref_port port_name="SIG3" />
</portgroup>
<constraint>
 <delay  port_name="CLK" min="10" typ="12" max="15" />
 <delay  port_id="D3"  typ="5" />
 <delay  group_name="BUS"  min="50" typ="55" max="60"/>
</constraint>
```

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8.2.4.11.5 The <skew> element

8.2.4.11.5.1 General

The <skew> element defines the skew constraint for signals that input and output from the specified port.

```
<skew
            { port_name="name_of_port" |
             port_id="identifier_of_port" |
             group_name="name_of_port_group" }
            [ reference_port_name="name_of_referenced_port" |
            reference_port_id="identifier_of_referenced_port" ]
            [min="minimum_time"]
            [max="maximum_time"]
/>
```

The port shall be specified with either the port name (port_name), port identifier (port_id), or group name (group_name) attribute.

When the reference signal is specified, the skew constraint is defined by a maximum time (max) and a minimum time (min). In this case, the specified maximum and minimum times are based on the propagation time of the reference signal that inputs or outputs from the specified reference port (reference_port_name, reference_port_id). The propagation time of signals having a skew constraint is required to close within the minimum through the maximum time (see Figure 26).

```
<portgroup name="skewset1">
  <ref_port  name="port1" />
  <ref_port  name="port2" />
  <ref_port  name="port3" />
</portgroup>
<skew   group_name="skewset1"  reference_port_name="port0"
            min="-5" max="10" />
```

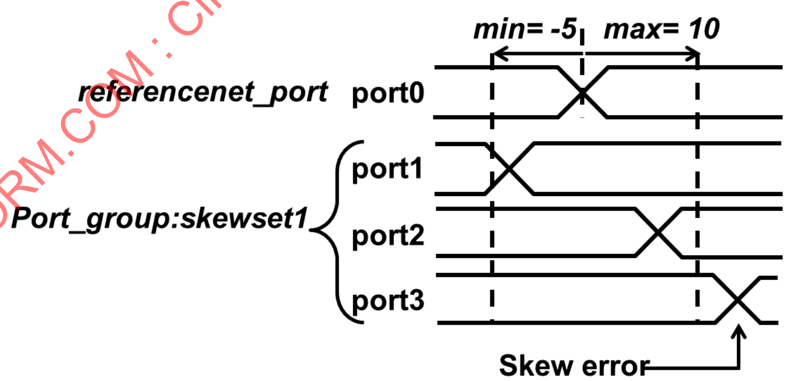

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Figure 26—Sample of skew constraint with min and max attributes

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When the reference signal is not specified, the skew constraint is defined by either the maximum time (`max`) or minimum time (`min`). If the maximum time is defined, a signal having the slowest propagation time is used as the reference signal (see Figure 27).

```
<portgroup name="skewset2">
  <ref_port name="port4" />
  <ref_port name="port5" />
  <ref_port name="port6" />
</portgroup>
<skew   group_name="skewset2"   max=“10" />
```

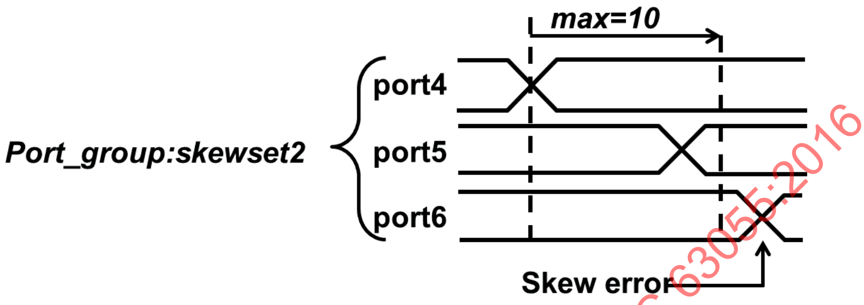

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Figure 27 —Sample of skew constraint with only `max` attribute

If only a minimum time (`min`) is defined, a signal having the fastest propagation time is used as the reference signal (see Figure 28).

```
<portgroup name="skewset3">
  <ref_port name="port7" />
  <ref_port name="port8" />
  <ref_port name="port9" />
</portgroup>
<skew   group_name="skewset3"   min="-10" />
```

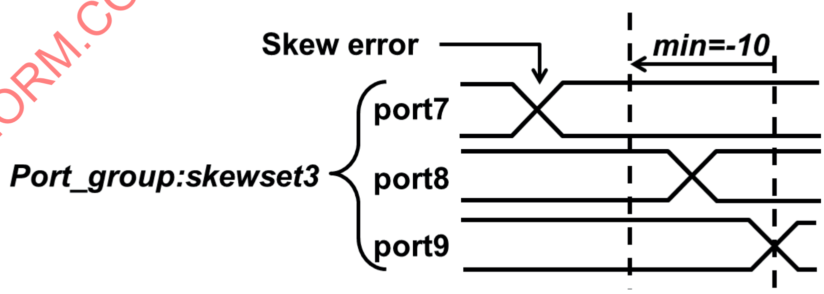

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Figure 28 —Sample of skew constraint with only `min` attribute

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8.2.4.11.5.2 Attribute definitions

The attributes of the <skew> element are defined as follows.

port_name

This attribute specifies the name of a predefined port for inputting and outputting a signal that requests a skew constraint. The specified port shall be defined at the <port> element in the same <socket> element. The port_name attribute shall not be used with the port_id and group_name attributes.

port_id

This attribute specifies the identifier of a predefined port for inputting and outputting a signal that requests a skew constraint. The specified port shall be defined at the <port> element in the same <socket> element. The port_id attribute shall not be used with the port_name and group_name attributes.

group_name

This attribute specifies the name of a group that includes ports for inputting and outputting a signal that requests a skew constraint. The specified port group shall be defined at the <portgroup> element in the same <socket> element. The group_name attribute shall not be used with the port_name and port_id attributes.

reference_port_name

This attribute specifies the name of a predefined port for inputting and outputting a reference signal of a skew constraint. The specified port shall be defined at the <port> element in the same <socket> element. The reference_port_name attribute shall not be used with the reference_port_id attribute.

reference_port_id

This attribute specifies the identifier of a predefined port for inputting and outputting a reference signal of a skew constraint. The specified port shall be defined at the <port> element in the same <socket> element. The reference_port_name attribute shall not be used with the reference_port_id attribute.

min
max

The max and min attributes specify maximum and minimum time, respectively. When a reference signal is specified by the reference_port_name or reference_port_id attribute, the min and max attributes shall be used together. When a reference signal is not specified, either the min or max attribute shall be used. The unit of minimum and maximum time is defined by the <time> element in the <unit> element.

8.2.4.11.5.3 Example

Assume that a semiconductor designer delivers a chip with a differential skew constraint. The following code is an example of a differential skew constraint of 5 ps. If a package designer routes the differential signal in 100 ps and 95 ps delays, the skew constraint to the printed-circuit-board designer would be 5 ps.

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```
<portgroup name="CK">
   <ref_port name="CKP" />
   <ref_port name="CKN" />
</portgroup>
<skew group_name="CK"  max="10" />
```

If the package designer routes the differential signal in 100 ps and 95 ps delays, the minimum and maximum skew constraints for board designers would be -5 ps and 15 ps, respectively. The following code and Figure 29 are examples of the skew constraint for the board designer.

```
<portgroup name="CK">
   <ref_port name="CKP" />
   <ref_port name="CKN" />
</portgroup>
<skew group_name="CK" reference_port_name="CKP" min="-5" max="15"
/>
```

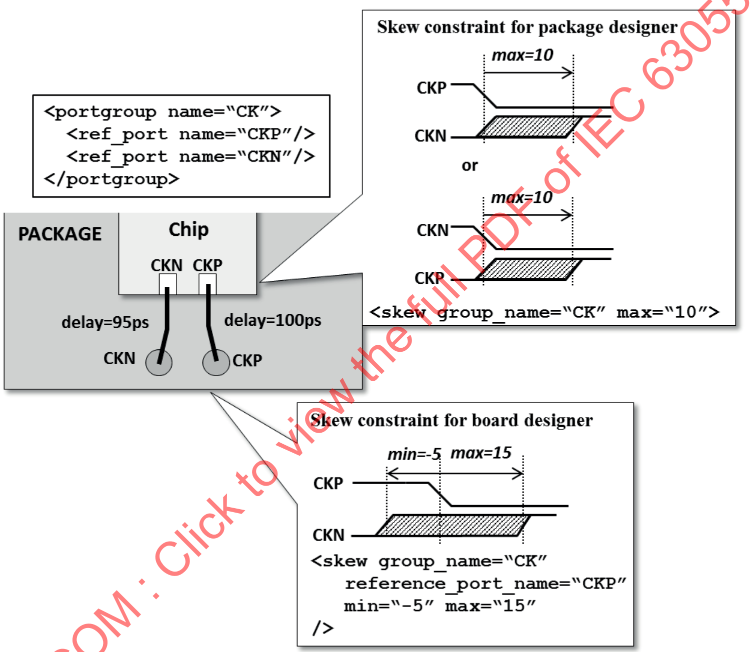

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Figure 29 —Example of a skew constraint for a differential clock

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8.2.4.11.6 The <guard_shield> element

8.2.4.11.6.1 General

The `<guard_shield>` element defines a signal used for a shield, and signals requiring a shield.

```
<guard_shield
              { port_name="name_of_port_requiring_shield" |
               port_id="identifier_of_port_requiring_shield" |
```

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```
              group_name="name_of_port_group_requiring_shield" }
             { shieldnet_port_name="name_of_port_using_shield"   |
              shieldnet_port_id="identifier_of_port_using_shield"   |
              shieldnet_port_group_name="name_of_port_group_using_shield" }
/>
```

For example, in the case of analog-digital mixed design, it would be better to shield the analog signal by analog ground. The `<guard_shield>` element is used to define the combination of shielding signals.

8.2.4.11.6.2 Attribute definitions

The attributes of the `<guard_shield>` element are defined as follows.

`port_name`

This attribute specifies the name of a predefined port for inputting and outputting a signal that requests a shield. The specified port shall be defined at the `<port>` element in the same `<socket>` element. The `port_name` attribute shall not be used with the `port_id` and `group_name` attributes.

`port_id`

This attribute specifies the identifier of a predefined port for inputting and outputting a signal that requests a shield. The specified port shall be defined at the `<port>` element in the same `<socket>` element. The `port_id` attribute shall not be used with the `port_name` and `group_name` attributes.

`group_name`

This attribute specifies the name of a group that includes ports for inputting and outputting a signal that requests a shield. The specified port group shall be defined at the `<portgroup>` element in the same `<socket>` element. If multiple ports with the same name exist, the signals that input or output from these ports shall be shielded. The `group_name` attribute shall not be used with the `port_name` and `port_id` attributes.

`shieldnet_port_name`

This attribute specifies the name of a predefined port for inputting and outputting a signal that is used for shielding. The specified port shall be defined at the `<port>` element in the same `<socket>` element. The `shieldnet_port_name` attribute shall not be used with the `shieldnet_port_id` and `shieldnet_port_group_name` attributes.

`shieldnet_port_id`

This attribute specifies the identifier of a predefined port for inputting and outputting a signal that is used for shielding. The specified port shall be defined at the `<port>` element in the same `<socket>` element. The `shieldnet_port_id` attribute shall not be used with the `shieldnet_port_name` and `shieldnet_port_group_name` attributes.

`shieldnet_port_group_name`

This attribute specifies the name of a group that includes ports for inputting and outputting a signal that is used for shielding. The specified port group shall be defined at the `<portgroup>` element in the same `<socket>` element. If multiple ports with the same name exist, any signals that are input or output from these ports can be used for shielding. The `shieldnet_port_group_name` attribute shall not be used with the `shieldnet_port_name` and `shieldnet_port_id` attributes.

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8.2.4.11.6.3 Example

The example of a guard shield in Figure 30 is represented by the following code. VSS is the guard net and CLK is the shielded net:

```
<guard_shield port_name="CLK" shieldnet_port_name="VSS" />
```

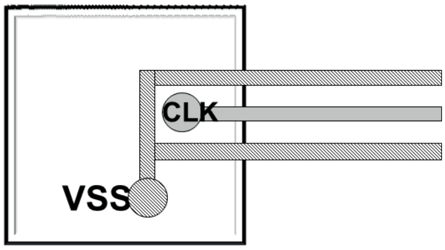

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Figure 30 —Example of a guard shield for a clock signal

8.2.5 The <specification> element

8.2.5.1 General

The `<specification>` element defines the specifications for the module itself, such as power consumption.

```
<specification>
            <power> element
</specification>
```

8.2.5.2 Element content

The `<specification>` element contains the following element:

```
<power>
```

8.2.5.3 The <power> element

8.2.5.3.1 General

The `<power>` element specifies the power consumption of the module.

```
<power>
            [min="minimum_power_consumption"]
            typ="typical_power_consumption"
            [max="maximum_power_consumption"]
/>
```

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8.2.5.3.2 Attribute definitions

The attributes of the `<power>` element are defined as follows.

`typ`

This attribute specifies the typical power consumption. The unit of power consumption is defined by the `<power>` element in the `<unit>` element.

`min`
`max`

These attributes specify the perturbation of power consumption. The `max` and `min` attributes are the maximum and minimum power consumption, respectively. The unit of power is defined by the `<power>` element in the `<unit>` element.

8.2.5.3.3 Example

The following is an example of the `<power>` element in use.

```
<specification>
      <power typ="1.0" />
</specification>
```

8.2.6 The <reference> element

8.2.6.1 General

The `<reference>` element defines the connection procedure between ports in the `<socket>` element and ports in a referenced file that is described by several formats.

```
<reference
              { xmlns:verilog="http://www.jeita.or.jp/LPB/verilog" |
                xmlns:VHDL="http://www.jeita.or.jp/LPB/VHDL" |
               xmlns:def="http://www.jeita.or.jp/LPB/def" |
               xmlns:spice="http://www.jeita.or.jp/LPB/spice" |
               xmlns:dxf="http://www.jeita.or.jp/LPB/dxf" |
               xmlns:gds="http://www.jeita.or.jp/LPB/gds" |
               xmlns:ibis="http://www.jeita.or.jp/LPB/ibis" |
               xmlns:xfl="http://www.jeita.or.jp/LPB/xfl" |
               xmlns:XML="http://www.jeita.or.jp/LPB/xml"
               xmlns:JLPB="http://www.jeita.or.jp/LPB/JLPB" }
              reffile="name_of_referenced_file"
              format="file_format"
              [type="file_type"]
              [distance="unit_of_length"]
              [scale="geometric_scale"]
>
              [<connection> element]…
</reference>
```

Some formats do not have the concept of I/O ports. In this case, coordinates that correspond to the position of the signal I/O are used to create the relationship with a port in the C-Format file. For example, the `<reference>` element can provide the position for I/O nodes of IBIS that does not have physical information.

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8.2.6.2 Attribute definitions

The attributes of the `<reference>` element are defined as follows.

```
xmlns:verilog="http://www.jeita.or.jp/LPB/verilog"
xmlns:VHDL="http://www.jeita.or.jp/LPB/VHDL"
xmlns:def="http://www.jeita.or.jp/LPB/def"
xmlns:spice="http://www.jeita.or.jp/LPB/spice"
xmlns:dxf="http://www.jeita.or.jp/LPB/dxf"
xmlns:gds="http://www.jeita.or.jp/LPB/gds"
xmlns:ibis="http://www.jeita.or.jp/LPB/ibis"
xmlns:xfl="http://www.jeita.or.jp/LPB/xfl"
xmlns:XML="http://www.jeita.or.jp/LPB/xml"
xmlns:JLPB="http://www.jeita.or.jp/LPB/JLPB"
```

This line is the namespace of the Extensible Markup Language (XML) [B2][6]. The namespace is used properly by the format of the referenced file. The corresponding namespaces and file formats are shown as follows:

`xmlns:verilog`

Verilog, standardized as IEEE Std 1364. It is used in the design and verification of digital circuits at gate-level or register-transfer level.

`xmlns:VHDL`

Very High Speed Integrated Circuits Hardware Description Language (VHDL) is standardized as IEEE Std 1076™-2008 [B3]. It is used in the design of digital and mixed-signal systems.

`xmlns:def`

Design Exchange Format (DEF), representing the physical layout of an integrated circuit in an ASCII format. It represents a netlist, component placements, and routing information.

`xmlns:spice`

Netlist for SPICE.

`xmlns:dxf`

Drawing Exchange Format (DXF). It is used for vector image files.

`xmlns:gds`

GDS II stream format. It is a database file format for data exchange of integrated circuits or integrated circuit layout artwork.

`xmlns:ibis`

IBIS. It is used by integrated circuit vendors to provide customers with information about the I/O buffers of a product.

`xmlns:XML`

[6] The numbers in brackets correspond to those of the bibliography in Annex A

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This name space is used to reference an external file that is defined in the XML language, such as an International Electrotechnical Commission (IEC) integrated circuit emission model (ICEM) or integrated circuit immunity model (ICIM) file.

`xmlns:xfl`

LPB G-Format.

`xmlns:JLPB`

LPB C-Format.

`reffile`

This attribute specifies the name of a file with which to make a relationship.

`format`

This attribute specifies the language of a reference file. The value shall be one of the following:

`VERILOG`	Verilog, standardized as IEEE Std 1364
`VHDL`	VHDL standardized as IEEE 1076-2008 [B3]
`DEF`	Design Exchange Format (DEF)
`SPICE`	Netlist for SPICE
`DXF`	Drawing Exchange Format (DXF)
`GDS`	GDS II stream format
`IBIS`	IBIS (Input/output Buffer Information Specification)
`XML`	XML language file.
`XFL`	LPB G-Format
`JLPB`	LPB C-Format

`type`

This attribute is used together with the `xmlns:XML` attribute. It specifies the kind of model file that is defined by XML language. The value shall be one of the following.

ICEM–CE, Integrated Circuit Electrical Model—Conducted Emission [B7]

ICEM–RE, Integrated Circuit Electrical Model—Radiated Emission [B8]

ICIM–CI, Integrated Circuit Immunity Model—Conducted Immunity [B9]

ICIM–RI, Integrated Circuit Immunity Model—Radiated Immunity [B10]

`distance`

This attribute specifies the unit system of distance for a reference file. If this attribute is not specified, the default of the reference file is used. The value shall be one of the following:

`pm`	picometer
`nm`	nanometer
`um`	micrometer
`mm`	millimeter
`m`	meter

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scale

This attribute specifies the scale range for a reference file. The scale range shall be more than zero. If this attribute is not specified, 1.0 is used as the default.

8.2.6.3 Element content

The <reference> element contains the following element:

<connection>

8.2.6.4 The <connection> element

8.2.6.4.1 General

The <connection> element defines the relationship between a <port> that is defined in the <socket> element and the I/O terminal of a reference file.

```
<connection
             socket_name="name_of_reference_socket"
             { port_name="name_of_referenced_port"  |
              port_id="identifier_of_referenced_port_id"  }
>
             [<verilog:ref_port> element]…
             [<VHDL:ref_port> element]…
             [<def:ref_port> element]…
             [<spice:ref_port> element]…
             [<dxf:ref_port> element]…
             [<gds:ref_port> element]…
             [<xfl:ref_port> element]…
             [<ibis:ref_port> element]…
             [<JLPB:ref_port> element]…
             [<xml:ref_port> element]…
</connection>
```

The connection scheme depends on the design language of the reference file. The following is a typical example.

The language in which a port is clearly defined as Verilog uses the combination of the “module name” and “port name” to define the relationship:

```
<connect socket_name="socket1" port_id="A1">
     <verilog:ref_port module="topmodule" portname="DQ1"/>
</connect>
```

In this example, A1 port in socket1 is associated with terminal DQ1 in topmodule of the Verilog description.

In the case of a SPICE netlist, the sub-circuit name and order of I/O node description are used to define the relationship:

```
<connect socket_name="socket1" port_id="A1">
    <spice:ref_port subckt="spicetop" portid="5"/>
</connect>
```

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In this example, A1 port in socket1 is associated with an I/O node that is defined in the fifth order in the sub-circuit spicetop.

8.2.6.4.2 Attribute definitions

The attributes of the <connection> element are defined as follows.

socket_name

> This attribute specifies the name of a socket that includes a port to make a relationship with the reference file. The specified socket shall be defined at the <socket> element in the same <module> element.

port_name

> This attribute specifies the name of a port to make a relationship with the reference file. The specified port shall be defined at the <port> element in the <socket> element, which is specified by the socket_name attribute. The port_name attribute shall not be used with the port_id attribute.

port_id

> This attribute specifies the identifier of a port to make a relationship with the reference file. The specified port shall be defined at the <port> element in the <socket> element, which is specified by the socket_name attribute. The port_id attribute shall not be used with the port_name attribute.

8.2.6.4.3 Element content

The <connection> element can contain the following elements:

```
<verilog:ref_port>
<VHDL:ref_port>
<def:ref_port>
<spice:ref_port>
<dxf:ref_port>
<gds:ref_port>
<xfl:ref_port>
<ibis:ref_port >
<JLPB:ref_port>
<xml:ref_port>
```

8.2.6.4.4 The <verilog:ref_port> element

8.2.6.4.4.1 General

The <verilog:ref_port> element is used to make a relationship with a Verilog language file.

```
<verilog:ref_port
        module="module_name_in_verilog_file"
        portname="port_name_in_verilog_file"
/>
```

In the case of a Verilog file, a relationship is created by the combination of module name and port name.

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8.2.6.4.4.2 Attribute definitions

The attributes of the `<verilog:ref_port>` are defined as follows.

`module`

This attribute specifies the name of a module in the reference Verilog file.

`portname`

This attribute specifies the name of a port in the reference Verilog file. The port shall be defined in the module that is specified by the `module` attribute.

8.2.6.4.4.3 Example

The following is an example of the `<verilog:ref_port>` element in use.

```
<reference
   xmlns:verilog="http://www.jeita.or.jp/LPB/verilog"
   reffile="XXXX.ver"
   format="VERILOG"
>
   <connection socket_name="socket1" port_id="A1">
      <verilog:ref_port  module="topmodule" portname="DQ1"/>
   </connection>
   <connection socket_name="socket1" port_id="A2">
      <verilog:ref_port module="topmodule"  portname="DQ2" />
   </connection>
   <connection socket_name="socket1" port_id="A3">
      <verilog:ref_port module="topmodule"  portname="DQ3" />
   </connection>
</reference>


[XXXX.ver]
  module topmodule(DQ1,DQ2,DQ3)
```

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8.2.6.4.5 The <VHDL:ref_port> element

8.2.6.4.5.1 General

The `<VHDL:ref_port>` element is used to make a relationship with the model file that is described by VHDL language.

```
<VHDL:ref_port
             entity="entity_name_in_VHDL_file"
             portname="port_name_in_VHDL_file"
/>
```

8.2.6.4.5.2 Attribute definitions

The attributes of the `<VHDL:ref_port>` element are defined as follows.

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`entity`

This attribute specifies the name of an entity in the reference VHDL file.

`portname`

This attribute specifies the name of a port in the reference VHDL file. The port shall be defined in the entity that is specified by the `entity` attribute.

8.2.6.4.5.3 Example

The following is an example of the <VHDL:ref_port> element in use.

```
<reference
   xmlns:VHDL="http://www.jeita.or.jp/LPB/VHDL"
   reffile="XXXX.vhd"
   format="VHDL"
>
   <connection socket_name="socket1" port_id="A1">
      <VHDL:ref_port  entity="topmodule" portname="DQ1"/>
   </connection>
   <connection socket_name="socket1" port_id="A2">
      <VHDL:ref_port entity="topmodule"  portname="DQ2" />
   </connection>
   <connection socket_name="socket1" port_id="A3">
      <VHDL:ref_port entity="topmodule"  portname="DQ3" />
   </connection>
</reference>
[XXXX.ver]
  module topmodule(DQ1,DQ2,DQ3)
  entity topmodule is
  port
  (
    DQ1       : out    std_logic;
    DQ2       : out    std_logic;
    DQ3       : out    std_logic;
  );
  end entity topmodule;
```

8.2.6.4.6 The <def:ref_port> element

8.2.6.4.6.1 General

The <def:ref_port> element is used to make a relationship with a DEF file.

```
<def:ref_port
              [comp="component_name_in_DEF_file"]
              pinname="pin_name_in_DEF_file"
/>
```

In the case of a DEF file, a relationship is created by using the pin name and/or component name.

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8.2.6.4.6.2 Attribute definitions

The attributes of the `<def:ref_port>` element are as follows.

`comp`

> This attribute specifies the name of a component that is defined in the COMPONENT section in the reference DEF file.

`pinname`

> This attribute specifies the name of a pin that is defined in the PINS section in the reference DEF file. Alternatively, it specifies the pin name of the component that is defined by the `comp` attribute.

8.2.6.4.6.3 Example

The following is an example of the `<def:ref_port>` element in use.

```
<reference
   xmlns:def="http://www.jeita.or.jp/LPB/def"
   reffile="XXXX.def"
   format="DEF"
>
   <connection socket_name="socket1" port_id="A1">
     <def:ref_port  comp="SBIO1" pinname="Z"/>
   </connection>
   <connection socket_name="socket1" port_id="A2">
     <def:ref_port  comp="SBIO2" pinname="Z"/>
   </connection>
   <connection socket_name="socket1" port_id="A3">
     <def:ref_port  comp="SBIO2" pinname="Z"/>
   </connection>
</reference>

[XXXX.def]
   COMPONENTS  100 ;
   -   SBIO1   io   ;
   -   SBIO2   io   ;
   -   SBIO3   io   ;
    .....
   END COMPONENTS


<reference xmlns:def=http://www.jeita.or.jp/LPB/def
   reffile="YYY.def"
   format="DEF"
>
   <connection socket_name="socket1" port_id="A1">
      <def:ref_port  pinname="PIN1"/>
   </connection>
   <connection socket_name="socket1" port_id="A2">
       <def:ref_port  pinname="PIN2"/>
   </connection>
   <connection socket_name="socket1" port_id="A3">
       <def:ref_port  pinname="PIN3"/>
   </connection>
</reference>

[YYYY.def]
```

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```
 PINS  10 ;
- PIN1  oDQ1 ;
- PIN2  oDQ2 ;
- PIN3  oDQ3;
  ...
END PINS
```

8.2.6.4.7 The <spice:ref_port> element

8.2.6.4.7.1 General

The `<spice:ref_port>` element is used to make a relationship with a SPICE netlist file.

```
<spice:ref_port
             subckt="name_of_subckt"
             portid="order_of_pins_in_subckt"
/>
```

In the case of SPICE, a relationship is created by the combination of the sub-circuit name and order of I/O node description. In the case of a SPICE netlist, the name of the sub-circuit (`.subckt`) and order of I/O node on the `.subckt` line are used to define the relationship.

8.2.6.4.7.2 Attribute definitions

The attributes of the `<spice:ref_port>` element are defined as follows.

`subckt`

This attribute specifies the name of a sub-circuit (`.subckt`) in the reference SPICE file.

`portid`

This attribute specifies the order of I/O nodes in the .subckt line. The value shall be an integer of 1 or more.

8.2.6.4.7.3 Example

The following is an example of the `<spice:ref_port>` element in use.

```
<reference
  xmlns:spice=”http://www.jeita.or.jp/LPB/spice”
  reffile="XXXX.sp"
  format="SPICE"
>
      <connection socket_name="socket1" port_id="A1">
        <spice:ref_port  subckt="top" portid="3"/>
      </connection>
      <connection socket_name="socket1" port_id="A2">
         <spice:ref_port  subckt="top" portid="2"/>
      </connection>
      <connection socket_name="socket1" port_id="A3">
         <spice:ref_port  subckt="top" portid="1"/>
      </connection>
</reference>
```

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```
[XXXXX.sp]
   subckt  top  p1  p2  p3 ;
```

8.2.6.4.8 The <dxf:ref_port> element

8.2.6.4.8.1 General

The `<dxf:ref_port>` element is used to make a relationship with a DXF file.

```
<dxf:ref_port
              x="x_coordinate"
              y="y_coordinate"
              dxf_layer="layer_name_in_DXF_file"
              mount=""
/>
```

The DXF language does not have a concept of the I/O terminal. Therefore, coordinates are used to create the relationship with a port in the C-Format file.

8.2.6.4.8.2 Attribute definitions

The attributes of the `<dxf:ref_port>` element are defined as follows.

`x`
`y`

These attributes specify the coordinates corresponding to the location of the input and output point of the signal.

`dxf_layer`

This attribute specifies the name of the layer on which the input and output point of the signal is placed.

`mount`

This attribute specifies the placement side of the input and output point of the signal. The value shall be either of the following:

`TOP` The I/O point is placed on the top side of the layer.
`BOTTOM` The I/O point is placed on the bottom side of the layer.

8.2.6.4.8.3 Example

The following is an example of the `<dxf:ref_port>` element in use.

```
<reference
   xmlns:dxf="http://www.jeita.or.jp/LPB/dxf"
   reffile="XXXX.dxf"
   format="DXF"
   distance="mm"
>
```

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```
        <connection socket_name="socket1" port_id="A1">
          <dxf:ref_port x="100" y="8978"   dxf_layer="L1"  module="TOP" />
        </connection>
        <connection socket_name="socket1" port_id="A2">
          <dxf:ref_port x="200" y="8978"   dxf_layer="L1"  module="TOP" />
        </connection>
        <connection socket_name="socket1" port_id="A3">
          <dxf:ref_port x="300" y="8978"   dxf_layer="L1"  module="TOP" />
        </connection>
</reference>
```

8.2.6.4.9 The <gds:ref_port> element

8.2.6.4.9.1 General

The `<gds:ref_port>` element is used to make a relationship with a GDS II stream format file.

```
<gds:ref_port
             x="x_coordinate"
             y="y_coordinate"
             gdx_layer="layer_number_in_GDS_file"
/>
```

The GDS II language does not have a concept of the I/O terminal. Therefore, coordinates are used to create the relationship with a port in the C-Format file.

8.2.6.4.9.2 Attribute definitions

The attributes of the `<gds:ref_port>` element are defined as follows.

`x`
`y`

These attributes specify the coordinates corresponding to the location of the input and output point of the signal.

`gds_layer`

This attribute specifies the number of layers on which input and output point of the signal is placed.

8.2.6.4.9.3 Example

The following is an example of the `<gds:ref_port>` element in use.

```
<reference
   xmlns:gds="http://www.jeita.or.jp/LPB/gds"
   reffile="XXXX.gds"
   format="GDS"
>
  <connection socket_name="socket1" port_id="A1">
      <gds:ref_port x="100" y="8978"   gds_layer="L1" />
  </connection>
  <connection socket_name="socket1" port_id="A2">
      <gdsref_port x="200" y="8978"   gds_layer="L1"  />
```

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```
  </connection>
  <connection socket_name="socket1" port_id="A3">
      <gds:ref_port x="300" y="8978"   gds_layer="L1" />
  </connection>
</reference>
```

8.2.6.4.10 The <xfl:ref_port> element

8.2.6.4.10.1 General

The `<xfl:ref_port>` element is used to make a relationship with an LPB G-Format file.

```
<xfl:ref_port
             component="component_name_in_XFL_file"
             pinname="pin_name_in_XFL_file"
/>
```

8.2.6.4.10.2 Attribute definitions

The attributes of the `<xfl:ref_port>` element are defined as follows.

`component`

This attribute specifies the name of a component that is defined in the **`.component`** section in the reference G-Format file.

`pinname`

This attribute specifies the pin name of the component that is defined in the `part` section in the references G-Format file.

8.2.6.4.10.3 Example

The following is an example of the `<xfl:ref_port>` element in use.

```
<reference
   xmlns:xfl="http://www.jeita.or.jp/LPB/xfl"
   reffile="XXXX.xfl"
   format="XFL"
>
 <connection socket_name="socket1" port_id="A1">
      <xfl:ref_port component="NEWLSIDIE" pinname="1" />
 </connection>
 <connection socket_name="socket1" port_id="A2">
      <xfl:ref_port component="NEWLSIDIE" pinname="2" />
 </connection>
 <connection socket_name="socket1" port_id="A3">
      <xfl:ref_port component="NEWLSIDIE" pinname="3" />
 </connection>
</reference>

 [XXXX.xfl]
.part
DIE R -13.5 -13.5 13.5 13.5 0 S 0 {
```

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```
    1 -4 -5 B 4
    2  -3 -5 B 4
    3 -2  -5 B 4
            :
}
.end part
.component
   NEWLSIDIE     DIE      0 0 1 0
.end component
```

8.2.6.4.11 The <ibis:ref_port> element

8.2.6.4.11.1 General

The `<ibis:ref_port>` element is used to make a relationship with an IBIS file.

```
<ibis:ref_port
             component="component_name_in_IBIS_file"
             signal_name="signal_name_in_IBIS_file"
/>
```

8.2.6.4.11.2 Attribute definitions

The attributes of the `<ibis:ref_port>` element are defined as follows.

`component`

> This attribute specifies the name of a component that is defined in the `[Component]` line in the reference IBIS file.

`signal_name`

> This attribute specifies the `signal_name` that is defined in the reference IBIS file.

8.2.6.4.11.3 Example

The following is an example of the `<ibis:ref_port>` element in use.

```
<reference
  xmlns:ibis="http://www.jeita.or.jp/LPB/ibis"
  reffile="XXXX.ibs"
  format="IBIS"
>
   <connection socket_name="socket1" port_id="A1">
      <ibis:ref_port  component="DDR3-1Gbx16" signal_name="Vddq"/>
   </connection>
   <connection socket_name="socket1" port_id="A2">
       <ibis:ref_port component="DDR3-1Gbx16"  signal_name="DQU5" />
   </connection>
   <connection socket_name="socket1" port_id="A3">
       <ibis:ref_port component="DDR3-1Gbx16"  signal_name="DQU7" />
   </connection>
</reference>
```

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```
XXXX.ibs

[IBIS ver]        4.2
[File name]      XXXXX.ibs
 .......
[Component]      DDR3-1Gbx16
[Manufacturer]    JEITA_FACT
[Package]
| variable        typ                 min                 max
R_pkg             0.5                 0.4                 0.6
L_pkg             1.5nH              1.0nH              2.0nH
C_pkg             0.4pF              0.2pF              0.6pF
|
[Pin]  signal_name       model_name     R_pin        L_pin         C_pin
A1     Vddq              POWER
A2     DQU5              DQ_MODEL       0.58         1.9nH         0.58pF
A3     DQU7              DQ_MODEL       0.57         1.85nH        0.57pF
 ....
```

8.2.6.4.12 The <JLPB:ref_port> element

8.2.6.4.12.1 General

The <JLPB:ref_port> element is used to make a relationship with an LPB Format C-Format file.

```
<JLPB:ref_port
              module="module_name_in_LPB_CFormat"
              socket="socket_name_in_LPB_CFormat"
              [port_name="port_name_in_LPB_CFormat" |
              port_id="port_identifier_in_LPB_CFormat" ]
/>
```

8.2.6.4.12.2 Attribute definitions

The attributes of the <JLPB:ref_port> element are defined as follows.

module

This attribute specifies the name of a module that is defined in the <module> element in the reference C-Format file.

socket

This attribute specifies the name of a socket that is defined in the <socket> element in the reference C-Format file. The socket shall be defined in the module that is specified by the module attribute.

port_name

This attribute specifies the name of a port that is defined in the <port> element in the reference C-Format file. The port shall be defined in the socket that is specified by the socket attribute. The port_name attribute shall not be used with the port_id attribute.

port_id

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This attribute specifies the identifier of a port that is defined in the `<port>` element in the reference C-Format file. The port shall be defined in the socket that is specified by the `socket` attribute. The `port_id` attribute shall not be used with the `port_name` attribute.

8.2.6.4.13 The <xml:ref_port> element

8.2.6.4.13.1 General

The `<xml:ref_port>` element is used to make a relationship with the model file that is described by the XML language.

```
<xml:ref_port
             port_path="xpath"
/>
```

The path to nodes in the model file is expressed using XML Path Language (`xpath`).

8.2.6.4.13.2 Attribute definitions

The attributes of the `<xml:ref_port>` element are defined as follows.

`port_path`

This attribute specifies a path to an I/O node in the referenced model file. The path is expressed by XML Path Language version 1.0.

8.2.6.4.13.3 Example

The following is an example of the `<xml:ref_port>` element in use.

```
<reference
  xmlns:XML="http://www.jeita.or.jp/LPB/xml"
  reffile="ICEMCE.xml"
  format="XML"
  type="ICEM-CE"
>
   <connection socket_name="socket1" port_id="A1">
      <xml:ref_port port_path="/Cemodel/Lead_definitios/Lead[@Id='3']"/>
   </connection>
   <connection socket_name="socket1" port_id="A2">
      <xml:ref_port port_path="/Cemodel/Lead_definitios/Lead[@Id='4']"/>
   </connection>
   <connection socket_name="socket1" port_id="A3">
      <xml:ref_port port_path="/Cemodel/Lead_definitios/Lead[@Id='5']"/>
   </connection>
</reference>
```

```
[ICEMCE.xml]

<Cemodel>
     ...
  <Lead_definitions>
```

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```
    <Lead Id="3" Name="Vssq" Mode="GND"/>
    <Lead Id="3" Name="DQU5" Mode="external"/>
    <Lead Id="3" Name="DQU7" Mode="external"/>

        ...
  </Lead_definitions>
    ...
</Cemodel>
```

8.3 The <component> element

8.3.1 General

The <component> element instantiates modules and gives physical information, such as placement.

```
<component>
              [<placement> element]…
</component>
```

If multiple <module> elements are defined, the <component> element defines the location of parts in the first defined module.

8.3.2 Element content

The <component> element contains the following element:

<placement>

8.3.3 The <placement> element

8.3.3.1 General

The <placement> element defines how to place the module.

```
<placement
              ref_module="name_of_referenced_module"
              inst="instance_name"
              [distance="unit_of_length"]
              [angleunit="unit_of_angle"]
              [scale="geometrical_scale"]
              x="x_coordinate"
              y="y_coordinate"
              [z="z_coordinate"]
              [flip="flip_type"]
              [angle="rotation_angle"]
              [mount="mount_type"]
/>
```

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8.3.3.2 Attribute definitions

The attributes of the `<placement>` element are defined as follows.

`ref_module`

This attribute specifies the name of a predefined module for placement.

`inst`

This attribute specifies the instance name of a module. The instance name shall be unique in the same file.

`distance`

This attribute specifies the unit of the x/y coordinate. If this attribute is not specified, the unit that is defined at the `<distance>` element in the `<unit>` element is used. The value shall be one of the following:

`pm`	picometer
`nm`	nanometer
`um`	micrometer
`mm`	millimeter
`m`	meter

`angleunit`

This attribute specifies the unit of an angle. If this attribute is not specified, the unit that is defined at the `<angle>` element in the `<unit>` element is used. The value shall be either of the following:

`degree`
`radian`

`scale`

This attribute specifies the scale rate of distance. The scale rate shall be more than zero. If this attribute is not specified, 1.0 is used as the default.

`x`
`y`

These attributes specify the location of the reference point of the module. The `x` and `y` attributes specify the x-coordinate and y-coordinate, respectively.

`z`

This attribute specifies the z-coordinate of the module, namely, the height of the module from the top layer as shown in Figure 31. If this attribute is not specified, zero is set as the default.

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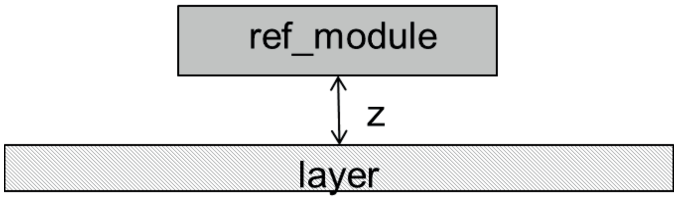

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Figure 31 —Explanatory drawing of the z-coordinate of a module

`flip`

This attribute specifies the type of flip. The value shall be either of the following:

`X`	X-flip flipping about the X-axis
`Y`	Y-flip flipping about the Y-axis

Figure 32 shows examples of an `X-flip` and a `Y-flip`.

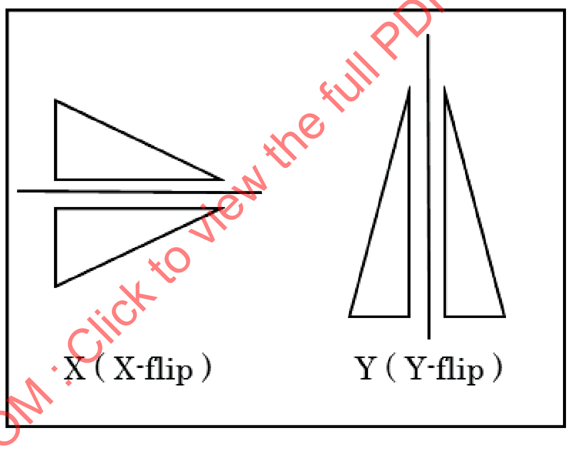

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Figure 32 —Explanatory drawing an X-FLIP and a Y-FLIP

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`angle`

This attribute specifies the angle of the counterclockwise rotation with respect to the reference point of the module. If an angle is not specified, zero is set as the default.

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`mount`

This attribute specifies the placement side of the module. The value shall be either of the following:

`TOP` The `module` is placed on the top side.
`BOTTOM` The module is placed on the bottom side.

Figure 33 shows an example of a `TOP` mount and a `BOTTOM` mount.

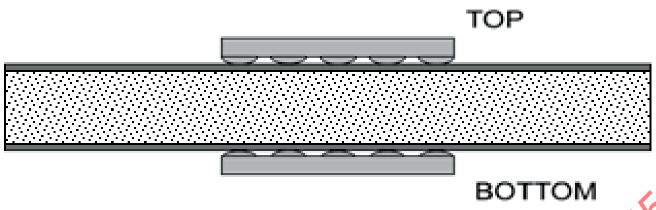

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Figure 33—Explanatory drawing of TOP and BOTTOM module mounting

8.3.3.3 Example

The following is an example of the `<placement>` element in use.

```
<component>
  <placement ref_module="CAP0603B" inst="C10"
             x="-8584.7" y="-4104.9" mount="BOTTOM" />
  <placement ref_module="CAP0603B" inst="C11"
             x="-8584.7" y="-6355.9" mount="BOTTOM" />
  <placement ref_module="CAP1005B" inst="C12"
             x="26092.5" y="37686.8" angle="90" mount="BOTTOM" />
  <placement ref_module="CAP1005B" inst="C13"
             x="30005.4" y="37686.8" angle="90" mount="BOTTOM" />
  <placement ref_module="CAP1005B" inst="C14"
             x="34659.6" y="37686.8" angle="90" mount="BOTTOM" />
  <placement ref_module="CAP1005B" inst="C15"
             x="40178.8" y="37686.8" angle="90" mount="BOTTOM" />

  <placement ref_module="RAS8" inst="RAS8_RN2"
             x="25477.7" y="15729.6" angle="270" mount="TOP" />
  <placement ref_module="RAS8" inst="RAS8_RN4"
             x="43929.3" y="6225.3" angle="270" mount="TOP" />
  <placement ref_module="REGULATOR" inst="REGULATOR"
             x="-12598" y="10183.9" mount="TOP" />
  <placement ref_module="SOC_PKG" inst="SOC"
             x="400" y="-6500" mount="TOP" />
  <placement ref_module="XTAL" inst="XTAL"
             x="-6285.9" y="26473" mount="TOP" />
</component>
```

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9. R-Format

9.1 R-Format file structure

The content of the R-Format file consists of one <header> element, one <global> element, at least one <Physicaldesign> element, and zero or one <Constraintrule> element. These elements shall be specified in the following order:

```
<LPB_RFORMAT>
             <header> element
             <global> element
             { <Physicaldesign> element }…
             [ <Constraintrule> element ]
</LPB_RFORMAT>
```

9.2 The <Physicaldesign> element

9.2.1 General

The <Physicaldesign> element specifies the physical parameters, such as the materials of the conductor and dielectric, layer stackup, design rules, via, bonding wire, ball, and mold.

```
<Physicaldesign
             name="design_rule_name"
>
             [<default/>]
             [<material_def> element]
             [<layer_def> element]
             [<spacing_def> element]
             [<pitch_def> element]
             [<bondingwire_def> element]
             [<ball_def> element]
             [<mold> element]
             [<condctor_struct> element]
</Physicaldesign>
```

The <Physicaldesign> element consists of the name attribute, zero or one <default> element, zero or one <material_def> element, zero or one <layer_def> element, zero or one <spacing_def> element, zero or one <pitch_def> element, zero or one <bondingwire_def> element, zero or one <ball_def> element, zero or one <mold> element, and zero or one <conductor_struct> element.

9.2.2 Attribute definition

The attribute of the <Physicaldesign> element is defined as follows.

name

This attribute specifies the name of the design rule.

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9.2.3 Element content

The <Physicaldesign> element can contain the following elements:

```
<default/>
<material_def>
<layer_def>
<spacing_def>
<pitch_def>
<bondingwire_def>
<ball_def>
<mold>
<condctor_struct>
```

9.2.4 Example

The following is an example of the <Physicaldesign> element in use.

```
<Physicaldesign name="default_rule">
   <default/>
   <material_def>
      <conductor
         material="COPPER"
         volume_resistivity="1.68e-8"
         temperature="20"
      />
   </material_def>
   <layer_def>
      <layer name="L1"
         type="conductor"
         thickness="10"
         conductor_material="COPPER">
         <line_width min="40"/>
      </layer>
   </layer_def>
   <spacing_def>
      <layer name="L1">
         <line_to_line space="40"/>
         <line_to_via via="VIA_L1_L2" space="40"/>
         <line_to_polygon space="55"/>
      </layer>
   </spacing_def>
   <bondingwire_def>
      <bondingwire name="WIREBOND1" diameter="20" material="GOLD">
         <forward horizontal_length="0" vertical_length="100"/>
         <forward vertical_length="0" horizontal_ratio="0.125"/>
         <length min="500" max="3000"/>
      </bondingwire>
   </bondingwire_def>
   <ball_def>
      <ball name="BGA_Ball" material="SOLDER">
         <frustum height="250" diam1="300" diam2="300"/>
      </ball>
   </ball_def>
   <mold width="12000" depth="12000" height="600" material="RESIN" />
   <conductor_struct>
      <trapezodial_angle layer="L1" angle="60"/>
      <surface_roughness layer="L1" UP_RMS="2" DOWN_RMS="5"/>
   </conductor_struct>
</Physicaldesign>
```

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9.2.5 The <default> element

The <default> element specifies the <Physicaldesign> element as a default design rule of the whole area.

```
<default/>
```

9.2.6 The <material_def> element

9.2.6.1 General

The <material_def> element specifies the material of the conductor and dielectric.

```
<material_def>
              [<conductor> element]…
              [<dielectric> element]…
</material_def>
```

The <material_def> element consists of zero or more <conductor> elements and zero or more <dielectric> elements.

9.2.6.2 Element content

The <material_def> element can contain the following elements:

```
<conductor>
<dielectric>
```

9.2.6.3 Example

The following is an example of the <material_def> element in use.

```
<material_def>
    <conductor
      material="COPPER"
      volume_resistivity="1.68e-8"
      temperature="20"/>
    <conductor
      material="GOLD"
      volume_resistivity="2.33e-8"
      temperature="20"/>
    <conductor
      material="SOLDER"
      volume_resistivity="2.17e-7"
      temperature="20"/>
    <dielectric
      material="FR-4"
      permittivity="4.5"
      tan_delta="0.035" frequency="1e9"/>
    <dielectric
      material="RESISTOR_INK"
```

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```
      permittivity="4.5"
      tan_delta="0.035"
      frequency="1e9"/>
    <dielectric
      material="REGIN"
      permittivity="4.5"
      tan_delta="0.035"
      frequency="1e9"/>
</material_def>
```

9.2.6.4 The <conductor> element

9.2.6.4.1 General

The <conductor> element specifies the characteristics of the conductor.

```
<conductor
              material="material_name"
              volume_resistivity="resistivity"
              [temperature="temperature"]
/>
```

The <conductor> element consists of the material attribute, the volume_resistivity attribute, and the optional temperature attribute.

9.2.6.4.2 Attribute definitions

The attributes of the <conductor> element are defined as follows.

material

This attribute specifies the name of the conductor.

volume_resistivity

This attribute specifies the volume resistivity of the conductor.

temperature

This attribute specifies the temperature conditions when the volume resistivity of the conductor is measured.

9.2.6.4.3 Example

The following is an example of the <conductor> element in use.

```
<conductor
              material="COPPER"
              volume_resistivity="1.68e-8"
```

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```
                temperature="20"
/>
```

9.2.6.5 The <dielectric> element

9.2.6.5.1 General

The `<dielectric>` element specifies the characteristics of the dielectric.

```
<dielectric
                material="material_name"
                permittivity="permittivity"
                [tan_delta="loss_tangent"]
                [frequency="frequency"]
/>
```

The `<dielectric>` element consists of the `material` attribute, the `permittivity` attribute, the optional `tan_delta` attribute, and the optional `frequency` attribute.

9.2.6.5.2 Attribute definitions

The attributes of the `<dielectric>` element are defined as follows.

`material`

This attribute specifies the name of the dielectric material.

`permittivity`

This attribute specifies the dielectric constant of the material.

`tan_delta`

This attribute specifies the dissipation factor of the material.

`frequency`

This attribute specifies the frequency that is used when the dielectric properties are measured.

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9.2.6.5.3 Example

The following is an example of the `<dielectric>` element in use.

```
<dielectric
                material="FR-4"
                permittivity="4.5"
```

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```
                tan_delta="0.035"
                frequency="1e9"
/>
```

9.2.7 The <layer_def> element

The `<layer_def>` element specifies the layer stackup from top to bottom.

```
<layer_def>
                {<layer> element}…
</layer_def>
```

The `<layer_def>` element consists of one or more `<layer>` elements.

9.2.7.1 Element content

The `<layer_def>` element contains the following element:

`<layer>`

9.2.7.2 Example

Figure 34 shows an example of the layer stackup that includes the conductor and dielectric layers.

```
<layer_def>
    <layer name="TOP_SR"
        type="dielectric"
        thickness="20"
        dielectric_material="RESISTOR_INK"/>
    <layer name="L1"
        type="conductor"
        thickness="10"
        conductor_material="COPPER"
    >
        <line_width min="40"/>
    </layer>
    <layer name="BU_1_2"
        type="dielectric"
        thickness="40"
        dielectric_material="FR-4"
    />
    <layer name="L2"
        type="conductor"
        thickness="10"
        conductor_material="COPPER"
    >
        <line_width min="50"/>
    </layer>
    <layer name="CORE"
        type="dielectric"
        thickness="100"
        dielectric_material="FR-4"
    />
    <layer name="L3"
        type="conductor"
        thickness="10"
        conductor_material="COPPER"
    >
```

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```
        <line_width min="50"/>
    </layer>
    <layer name="BU_3_4"
        type="dielectric"
        thickness="40"
        dielectric_material="FR-4"
    />
    <layer name="L4"
        type="conductor"
        thickness="10"
        conductor_material="COPPER"
    >
        <line_width min="40"/>
    </layer>
    <layer name="BOTTOM_SR"
         type="dielectric"
         thickness="20"dielectric_material="RESISTOR_INK"
    />
</layer_def>
```

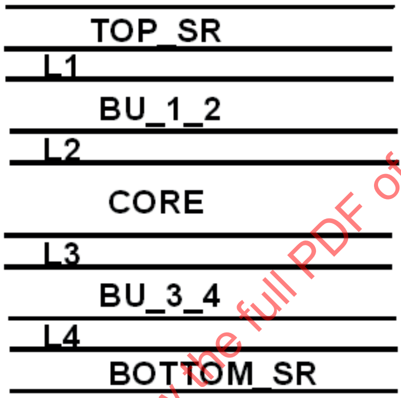

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Figure 34—Example of layer stackup

9.2.7.3 The <layer> element

9.2.7.3.1 General

The `<layer>` element specifies the layer name, type of the layer, thickness of the layer, material of the layer, and design rules for the line width and area.

```
<layer
              name="layer_name"
              type="layer_type"
              thickness="layer_thickness"
              [plate_thickness="plating_thickness"]
              [conductor_material="name_of_conductor_material"]
              [dielectric_material="name_of_dielectric_material"]
>
              [<line_width> element]
              [<area_limit> element]
</layer>
```

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The <layer> element consists of the name attribute, the type attribute, the thickness attribute, the optional plate_thickness attribute, the optional conductor_material attribute, the optional dielectric_material attribute, zero or one <line_width> element, and zero or one <area_limit> element.

9.2.7.3.2 Attribute definitions

The attributes of the <layer> element are defined as follows.

name

This attribute specifies the layer name.

type

This attribute specifies the type of the layer. The values are as follows:

dielectric	dielectric layer
conductor	conductor layer

thickness

This attribute specifies the layer thickness that is the overall thickness containing the plate_thickness, as shown in Figure 35.

plate_thickness

This attribute specifies the plating thickness that is contained in the thickness attribute, as shown in Figure 35.

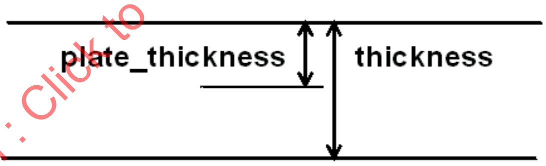

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Figure 35—Explanatory drawing of the relation of plate_thickness and thickness

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conductor_material

This attribute specifies the name of the conductor material.

dielectric_material

This attribute specifies the same of the dielectric material.

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9.2.7.3.3 Element content

The <layer> element can contain the following elements:

```
<line_width>
<area_limit>
```

9.2.7.3.4 Example

The following is an example of the <layer> element in use.

```
<layer
   name="TOP_SR"
   type="dielectric"
   thickness="20"
   dielectric_material="RESISTOR_INK"
/>
<layer
   name="L1"
   type="conductor"
   thickness="10"
   conductor_material="COPPER">
   <line_width min="40"/>
</layer>
<layer
   name="BU_1_2"
   type="dielectric"
   thickness="40"
   dielectric_material="FR-4"
/>
```

9.2.7.3.5 The <line_width> element

9.2.7.3.5.1 General

The <line_width> element specifies the design rules for the line width.

```
<line_width
        min="minimum_line_width"
        [max="maximum_line_width"]
/>
```

The <line_width> element consists of the min attribute and the optional max attribute.

9.2.7.3.5.2 Attribute definitions

The attributes of the <line_width> element are defined as follows.

min

This attribute specifies the minimum line width.

max

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This attribute specifies the maximum line width.

9.2.7.3.5.3 Example

The following is an example of the `<line_width>` element in use.

```
<line_width min="40" max="80" />
```

9.2.7.3.6 The <area_limit> element

9.2.7.3.6.1 General

The `<area_limit>` element specifies the minimum area rule.

```
<area_limit
             min="minimum_area"
/>
```

The `<area_limit>` element consists of the `min` attribute.

9.2.7.3.6.2 Attribute definition

The attribute of the `<area_limit>` element is defined as follows.

`min`

This attribute specifies the minimum metal area.

9.2.7.3.6.3 Example

The following is an example of the `<area_limit>` element in use.

```
<area_limit min="22500"/>
```

9.2.8 The <spacing_def> element

9.2.8.1 General

The `<spacing_def>` element defines the design rules of the space, such as the space between lines, between line and via, and between line and polygon.

```
<spacing_def>
             {<layer> element}…
</spacing>
```

The `<spacing_def>` element consists of one or more `<layer>` elements.

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9.2.8.2 Element content

The <spacing_def> element contains the following element:

<layer>

9.2.8.3 Example

The following is an example of the <spacing_def> element in use.

```
<spacing_def>
    <layer name="L1">
        <line_to_line space="40"/>
        <line_to_via via="VIA_L1_L2" space="40"/>
        <line_to_polygon space="55"/>
    </layer>
    <layer name="L2">
        <line_to_line space="50"/>
        <line_to_via  space="50"/>
        <line_to_via  space="50"/>
        <line_to_polygon space="55"/>
    </layer>
    <layer name="L3">
        <line_to_line space="50"/>
        <line_to_via space="50"/>
        <line_to_via via="VIA_L3_L4" space="50"/>
        <line_to_polygon space="55"/>
    </layer>
    <layer name="L4">
        <line_to_line space="40"/>
        <line_to_via  space="40"/>
        <line_to_polygon space="55"/>
    </layer>
</spacing_def>
```

9.2.8.4 The <layer> element

9.2.8.4.1 General

The <layer> element defines the design rules of the space, such as the space between lines, between line and via, and between line and polygon (see Figure 36).

```
<layer
             name="layer_name"
>
             [<line_to_line> element]
             [<line_to_via> element]…
             [<line_to_polygon> element]
</layer>
```

The <layer> element consists of the name attribute, zero or one <line_to_line> element, zero or more <line_to_via> elements, and zero or one <line_to_polygon> element.

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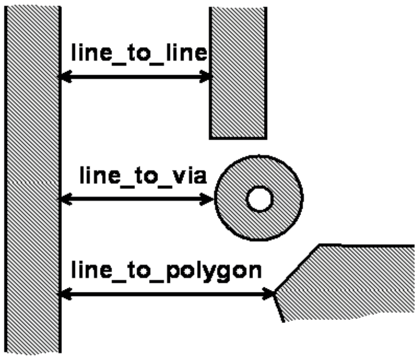

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Figure 36—Example of spacing rules

9.2.8.4.2 Attribute definition

The attribute of the `<layer>` element is defined as follows.

`name`

This attribute specifies the name of the layer.

9.2.8.4.3 Element content

The `<layer>` element can contain the following elements:

```
<line_to_line>
<line_to_via>
<line_to_polygon>
```

9.2.8.4.4 Example

The following is an example of the `<layer>` element in use.

```
<layer name="L1">
    <line_to_line    space="40"/>
    <line_to_via     via="VIA_L1_L2" space="40"/>
    <line_to_polygon space="55"/>
</layer>
<layer name="L2">
    <line_to_line    space="50"/>
    <line_to_via     space="50"/>
    <line_to_via     space="50"/>
    <line_to_polygon space="55"/>
</layer>
```

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9.2.8.4.5 The <line_to_line> element

9.2.8.4.5.1 General

The `<line_to_line>` element specifies the space between lines.

```
<line_to_line
             space="minimum_sacing"
/>
```

The `<line_to_line>` element consists of the `space` attribute.

9.2.8.4.5.2 Attribute definition

The attribute of the `<line_to_line>` element is defined as follows.

`space`

This attribute specifies the minimum space between lines.

9.2.8.4.5.3 Example

The following is an example of the `<line_to_line>` element in use.

```
<line_to_line space="50"/>
```

9.2.8.4.6 The <line_to_via> element

9.2.8.4.6.1 General

The `<line_to_via>` element specifies the space between line and via.

```
<line_to_via
             [via="identifier_of_padstack"]
             space="minimun_spacing"
/>
```

The `<line_to_via>` element consists of the optional `via` attribute and the `space` attribute.

9.2.8.4.6.2 Attribute definitions

The attributes of the `<line_to_via>` element are defined as follows.

`via`

This attribute specifies the padstack identifier of the via that is applied to the spacing rule.

`space`

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This attribute specifies the minimum space between line and via.

9.2.8.4.6.3 Example

The following is an example of the `<line_to_via>` element in use.

```
<line_to_via via="VIA_L1_L2" space="40"/>
```

9.2.8.4.7 The <line_to_polygon> element

9.2.8.4.7.1 General

The `<line_to_polygon>` element specifies the space between line and polygon.

```
<line_to_polygon
              space="minimum_spacing"
/>
```

The `<line_to_polygon>` element consists of the `space` attribute.

9.2.8.4.7.2 Attribute definition

The attribute of the `<line_to_polygon>` element is defined as follows.

`space`

This attribute specifies the minimum space between line and via.

9.2.8.4.7.3 Example

The following is an example of the `<line_to_polygon>` element in use.

```
<line_to_polygon space="55"/>
```

9.2.9 The <pitch_def> element

9.2.9.1 General

The `<pitch_def>` element specifies the pitch between center to center of vias.

```
<pitch_def>
              {<via_pitch> element}…
</pitch_def>
```

The `<pitch_def>` element consists of one or more `<via_pitch>` elements.

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9.2.9.2 Element content

The <pitch_def> element contains the following element:

```
<via_pitch>
```

9.2.9.3 Example

The following is an example of when the stack via cannot be used:

```
<pitch_def>
    <via_pitch via1="VIA_L1_L2" via2="VIA_L1_L2" pitch="250"/>
    <via_pitch     via1="VIA_L1_L2"     via2="VIA_L2_L3"     pitch="275"
samenet_pitch="225"/>
    <via_pitch via1="VIA_L2_L3" via2="VIA_L2_L3" pitch="300"/>
    <via_pitch     via1="VIA_L2_L3"     via2="VIA_L3_L4"     pitch="275"
samenet_pitch="225"/>
    <via_pitch via1="VIA_L3_L4" via2="VIA_L3_L4" pitch="250"/>
</pitch_def>
```

The following is an example of when the stack via can be used:

```
<pitch_def>
    <via_pitch via1="VIA_L1_L2" via2="VIA_L1_L2" pitch="250"/>
    <via_pitch     via1="VIA_L1_L2"     via2="VIA_L2_L3"     pitch="275"
stacked_offset="75"/>
    <via_pitch via1="VIA_L2_L3" via2="VIA_L2_L3" pitch="300"/>
    <via_pitch     via1="VIA_L2_L3"     via2="VIA_L3_L4"     pitch="275"
stacked_offset="75"/>
    <via_pitch via1="VIA_L3_L4" via2="VIA_L3_L4" pitch="250"/>
</pitch_def>
```

9.2.9.4 The <via_pitch> element

9.2.9.4.1 General

Figure 37 shows an example of a cross-section view of via structure. The <via_pitch> elements defines the design rule for via spacing, as shown in Figure 38.

```
<via_pitch
             via1="identifier_of_padstack"
             via2="identifier_of_padstack"
             pitch="minimum_pitch"
             [samenet_pitch="minimum_pitch_for_same_net"]
             [stacked_offset="acceptable_gap"]
/>
```

The <via_pitch> element specifies the pitch between vias from center to center (see Figure 38). The <via_pitch> element consists of the via1 attribute, the via2 attribute, the pitch attribute, the optional samenet_pitch attribute, and the optional stacked_offset attribute.

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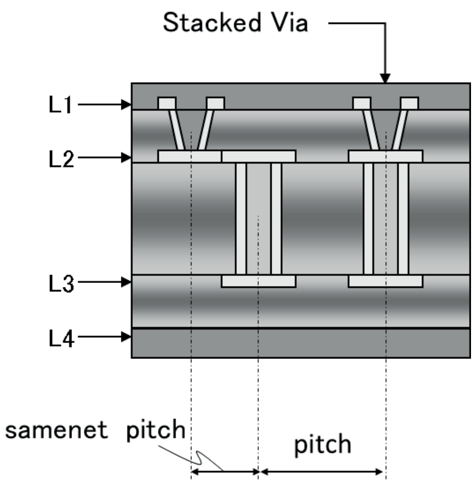

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Figure 37 —Example of via structure

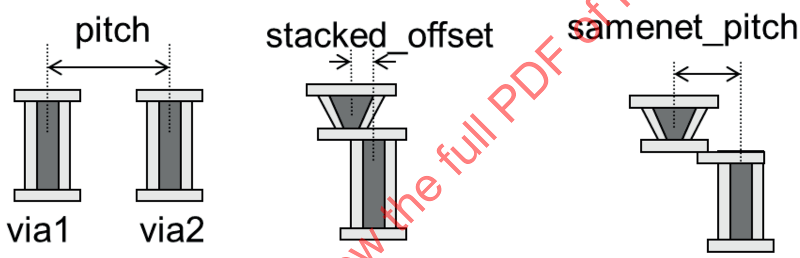

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Figure 38—Example of pitch between vias

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9.2.9.4.2 Attribute definitions

The attributes of the <via_pitch> element are defined as follows.

`via1`

This attribute specifies the padstack identifier of a via for which the via-pitch rule applies, as shown in Figure 38.

`via2`

This attribute specifies the padstack identifier of a via for which the via-pitch rule applies, as shown in Figure 38.

`pitch`

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This attribute specifies the minimum pitch between two vias on different nets, as shown in Figure 38.

samenet_pitch

This attribute specifies the minimum pitch between two vias in the same net, as shown in Figure 38.

stacked_offset

This attribute specifies the maximum acceptable gap between the centers of stacked vias, as shown in Figure 38.

9.2.9.4.3 Example

The following is an example of the <via_pitch> element in use.

```
<via_pitch
    via1="VIA_L1_L2"
    via2="VIA_L1_L2"
    pitch="250"
/>
<via_pitch
    via1="VIA_L1_L2"
    via2="VIA_L2_L3"
    pitch="275"
    samenet_pitch="225"
/>
<via_pitch
    via1="VIA_L1_L2"
    via2="VIA_L2_L3"
    pitch="275"
    stacked_offset="75"
/>
```

9.2.10 The <bondingwire_def> element

9.2.10.1 General

The <bondingwire_def> element specifies the shape and material of the bonding wire.

```
<bondingwire_def>
              {<bondingwire> element}…
</bondingwire_def>
```

The <bondingwire_def> element consists of one or more <bondingwire> elements.

9.2.10.2 Element content

The <bondingwire_def> element contains the following element:

<bondingwire>

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9.2.10.3 Example

The following is an example of the <bondingwire_def> element in use.

```
<bondingwire_def>
    <bondingwire name="WIREBOND1" diameter="20" material="GOLD">
         <forward horizontal_length="0" vertical_length="100"/>
         <forward vertical_length="0" horizontal_ratio="0.125"/>
         <length min="500" max="3000"/>
    </bondingwire>
</bondingwire_def>
```

9.2.10.4 The <bondingwire> element

9.2.10.4.1 General

The <bondingwire> element specifies the shape and material of the bonding wire.

```
<bondingwire
                name="wire_name"
                diameter="wire_diameter"
                [material="material_name"]
>
                [<forward> element]…
                [<backward> element]…
                [<length> element]
</bondingwire>
```

The <bondingwire> element consists of the name attribute, the diameter attribute, the optional material attribute, zero or more <forward> element, zero or more <backward> element, and zero or one <length> element.

9.2.10.4.2 Attribute definitions

The attributes of the <bondingwire> element are defined as follows.

name

This attribute specifies the name of the bonding wire.

diameter

This attribute specifies the diameter of the bonding wire.

material

This attribute specifies the material of the bonding wire.

9.2.10.4.3 Element content

The <bondingwire> element can contain the following elements:

<forward>

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```
<backward>
<length>
```

9.2.10.4.4 Example

Figure 39 shows an example of a JEDEC 4-point wire bonding shape that is defined by the corresponding `<bondingwire_def>` descriptions as follows:

JEDEC 4-point:

```
<bondingwire_def>
    <bondingwire name="WIREBOND1" diameter="20" material="GOLD">
        <forward horizontal_length="0" vertical_length="100"/>
        <forward vertical_length="0" horizontal_ratio="0.125"/>
        <length min="500" max="3000"/>
    </bondingwire>
</bondingwire_def>
```

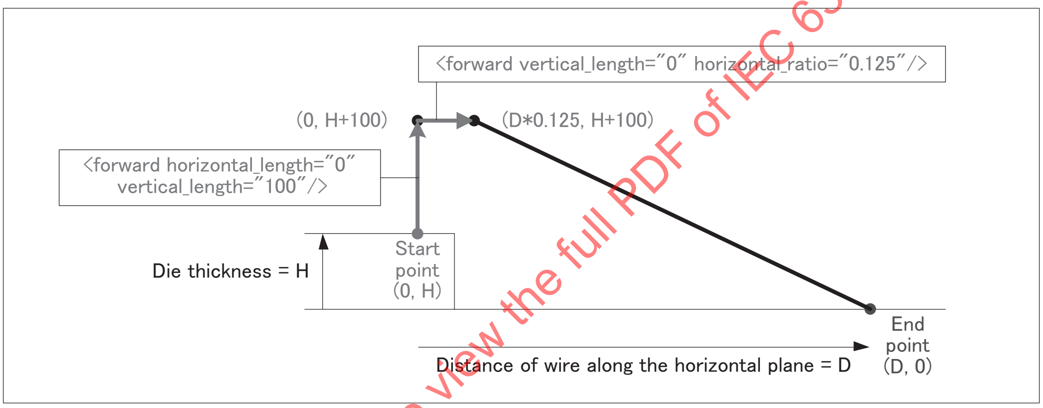

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Figure 39 —Example of bonding wire shape (JEDEC 4-point)

Figure 40 shows an example of a JEDEC 5-point wire bonding shape that is defined by the corresponding `<bondingwire_def>` descriptions as follows:

JEDEC 5-point:

```
<bondingwire_def>
    <bondingwire name="WIREBOND2" diameter="20" material="GOLD">
        <forward vertical_length="100" angle="80"/>
        <forward vertical_length="0" horizontal_ratio="0.125"/>
        <backward angle="20" horizontal_ratio="0.5"/>
        <length min="500" max="3000"/>
    </bondingwire>
</bondingwire_def>
```

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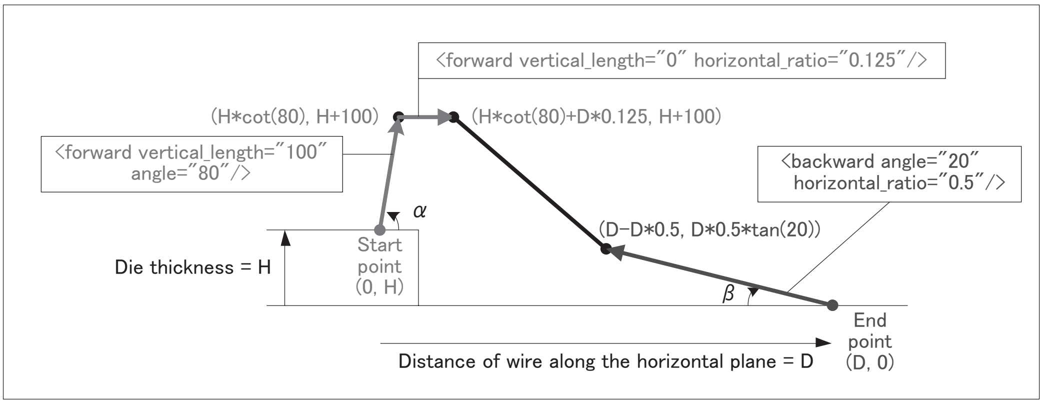

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Figure 40 —Example of bonding wire shape (JEDEC 5-point)

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9.2.10.4.5 The <forward> element

9.2.10.4.5.1 General

The `<forward>` element specifies the loop of the bonding wire from the die side.

```
<forward
        horizontal_length="horizontal_length"
        vertical_length="vertical_length"
        angle="die_side_angle"
        horizontal_ratio="horizontal_ratio"
/>
```

Some `<forward>` elements are specified from the first position to the second position toward the bonding finger (see Figure 41). The `<forward>` element consists of the optional `horizontal_length` attribute, the optional `vertical_length` attribute, the optional `angle` attribute, and the optional `horizontal_ratio` attribute.

9.2.10.4.5.2 Attribute definitions

The attributes of the `<forward>` element are defined as follows.

`horizontal_length`

This attribute specifies the horizontal length from the first position toward the bonding finger, as shown in Figure 41.

`vertical_length`

This attribute specifies the vertical length from the first position toward the bonding finger, as shown in Figure 41.

`angle`

This attribute specifies the angle from the first position toward the second position.

`horizontal_ratio`

This attribute specifies the ratio of the horizontal length (L1) and the total length (L) in Figure 41.

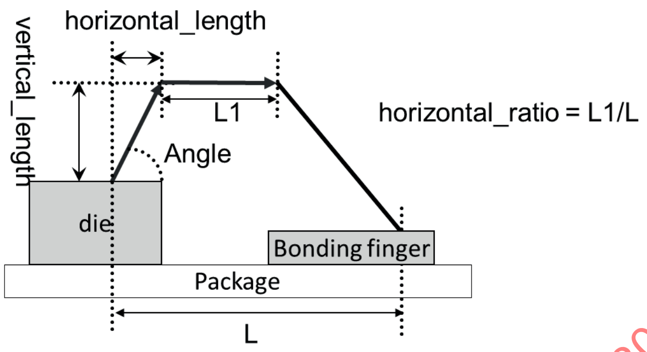

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Figure 41 —Explanatory drawing of the shape of a bonding wire

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9.2.10.4.5.3 Example

The following is an example of the `<forward>` element in use.

```
<forward horizontal_length="0" vertical_length="100"/>
<forward vertical_length="0"   horizontal_ratio="0.125"/>
```

9.2.10.4.6 The <backward> element

9.2.10.4.6.1 General

The `<backward>` element specifies the loop of the bonding wire from the bonding finger.

```
<backward
             horizontal_length="horizontal_length"
             vertical_length="vertical_length"
             angle="die_side_angle"
             horizontal_ratio="horizontal_ratio"
/>
```

Some `<backward>` elements are specified from the first position to the second position toward the die (see Figure 42). The `<backward>` element consists of the optional `horizontal_length` attribute, the optional `vertical_length` attribute, the optional `angle` attribute, and the optional `horizontal_ratio` attribute.

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9.2.10.4.6.2 Attribute definitions

The attributes of the `<backward>` element are defined as follows.

`horizontal_length`

This attribute specifies the horizontal length from the position toward the die, as shown in Figure 42.

`vertical_length`

This attribute specifies the vertical length from the first position toward the die, as shown in Figure 42.

`angle`

This attribute specifies the angle from the first position toward the die, as shown in Figure 42.

`horizontal_ratio`

This attribute specifies the ratio of the horizontal length (L1) and total length (L) in Figure 42.

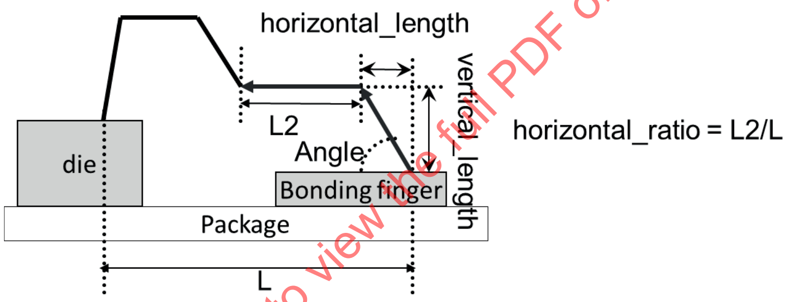

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Figure 42 —Explanatory drawing of the shape of a bonding wire

9.2.10.4.6.3 Example

The following is an example of the `<backward>` element in use.

```
<backward angle="20" horizontal_ratio="0.5"/>
```

9.2.10.4.7 The <length> element

9.2.10.4.7.1 General

The `<length>` element specifies the minimum length and maximum length of the bonding wire.

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```
<length
              min="minimum_length"
              max="maximum_length"
/>
```

The <length> element consists of the min attribute and the max attribute.

9.2.10.4.7.2 Attribute definitions

The attributes of the <length> element are defined as follows.

min

This attribute specifies the minimum length of the bonding wire.

max

This attribute specifies the maximum length of the bonding wire.

9.2.10.4.7.3 Example

The following is an example of the <length> element in use.

```
<length min="500" max="3000"/>
```

9.2.11 The <ball_def> element

9.2.11.1 General

The <ball_def> element specifies the material and shape of the solder ball.

```
<ball_def>
              {<ball> element}…
</ball_def>
```

The <ball_def> element consists of one or more <ball> element.

9.2.11.2 Element content

The <ball_def> element contains the following element:

<ball>

9.2.11.3 Example

The following is an example of the <ball_def> element in use.

```
<ball_def>
    <ball name="BGA_Ball" material="SOLDER">
```

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```
        <frustum height="250" diam1="300" diam2="300"/>
    </ball>
</ball_def>
```

9.2.11.4 The <ball> element

9.2.11.4.1 General

The `<ball>` element specifies the material and shape of the solder ball.

```
<ball
             name="ball_name"
             [material="material_name"]
>
             {<frustum> element>}…
</ball>
```

The `<ball>` element consists of the `name` attribute, the optional `material` attribute, and one or more `<frustum>` elements.

9.2.11.4.2 Attribute definitions

The attributes of the `<ball>` element are defined as follows.

`name`

This attribute specifies the name of the solder ball.

`material`

This attribute specifies the material of the solder ball.

9.2.11.4.3 Element content

The `<ball>` element contains the following element:

`<frustum>`

9.2.11.4.4 Example

The following is an example of the `<ball>` element in use.

```
<ball name="BGA_Ball" material="SOLDER">
   <frustum height="250" diam1="300" diam2="300"/>
</ball>
```

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9.2.11.4.5 The <frustum> element

9.2.11.4.5.1 General

The <frustum> element specifies the geometry of the solder ball.

```
<frustum
            height="height"
            diam1="diameter_of_top_side"
            diam2="diameter_of_bottom_side"
/>
```

The shape of the solder ball is given by a group of one or more frustums, as shown in Figure 43. The frustums are stacked up from top to bottom. The <frustum> element consists of the height attribute, the diam1 attribute, and the diam2 attribute.

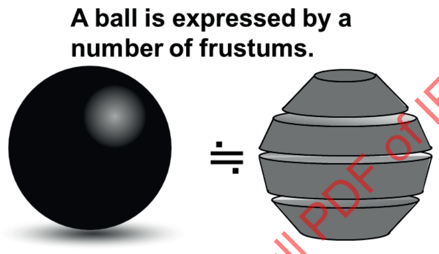

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Figure 43—Example of ball expression

9.2.11.4.5.2 Attribute definitions

The attributes of the <frustum> element are defined as follows.

height

This attribute specifies the height of the frustum.

diam1

This attribute specifies the diameter of the top side of the frustum.

diam2

This attribute specifies the diameter of the bottom side of the frustum.

Figure 44 shows the relationship of the dimensional attributes of a <frustum>: height, diam1, and diam2.

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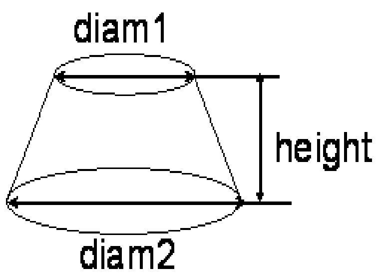

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Figure 44—Explanatory drawing of the shape of a frustum

9.2.11.4.5.3 Example

The following is an example of the `<frustum>` element in use.

9.2.12 <frustum height="250" diam1="300" diam2="300"/>The `<mold>` element

9.2.12.1 General

The `<mold>` element specifies the geometry and material of the package mold.

```
<mold
            width="width"
            depth="depth"
            height="height"
            material="material_name"
/>
```

The `<mold>` element consists of the `width` attribute, the `depth` attribute, the `height` attribute, and the `material` attribute. Figure 45 explains the `height` attribute of a `<mold>` element in relation to the layer stackup.

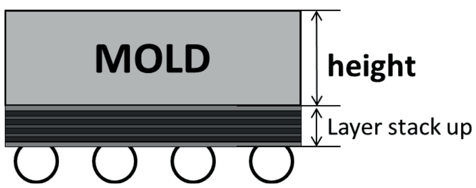

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Figure 45—Explanatory drawing of the `height` attribute of a mold

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9.2.12.2 Attribute definitions

The attributes of the `<mold>` element are defined as follows.

`width`

This attribute specifies the width of the package mold, as shown in Figure 46.

`depth`

This attribute specifies the depth of the package mold, as shown in Figure 46.

`height`

This attribute specifies the height of the package mold, as shown in Figure 46.

`material`

This attribute specifies the material of the package mold.

Figure 46 shows the `width`, `depth`, and `height` attributes of the `<mold>` element.

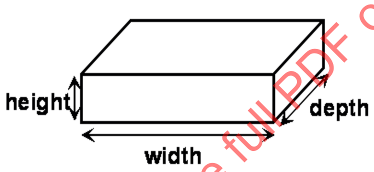

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Figure 46—Explanatory drawing of the shape of a mold

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9.2.12.3 Example

The following is an example of the `<mold>` element in use.

```
<mold
    width="12000"
    depth="12000"
    height="600"
    material="RESIN"
/>
```

9.2.13 The <conductor_struct> element

9.2.13.1 General

The `<conductor_struct>` element specifies the cross-section of the conductor.

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```
<conductor_struct>
              [<trapezoidal_angle> element]…
              [<surface_roughness> element]…
</conductor_struct>
```

The cross-sectional shape of the conductor is specified as trapezoidal with a specified angle. The `<conductor_struct>` element consists of zero or more `<trapezoidal_angle>` elements and zero or more `<surface_roughness>` elements.

9.2.13.2 Element content

The `<conductor_struct>` element can contain the following elements:

```
<trapezoidal_angle>
<surface_roughness>
```

9.2.13.3 Example

The following is an example of the `<conductor_struct>` element in use.

```
<conductor_struct>
    <trapezodial_angle layer="L1" angle="60"/>
    <trapezodial_angle layer="L4" angle="-60"/>
    <surface_roughness layer="L1" UP_RMS="2" DOWN_RMS="5"/>
    <surface_roughness layer="L4" UP_RMS="5" DOWN_RMS="2"/>
</conductor_struct>
```

9.2.13.4 The <trapezoidal_angle> element

9.2.13.4.1 General

The `<trapezoidal_angle>` element specifies the cross-sectional shape of the conductor.

```
<trapezoidal_angle
              layer="layer_name"
              angle="angle"
/>
```

The `<trapezoidal_angle>` element consists of the `layer` attribute and the `angle` attribute.

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9.2.13.4.2 Attribute definitions

The attributes of the `<trapezoidal_angle>` element are defined as follows.

`layer`

This attribute specifies the name of the conductor layer that is specified in the `<layer_def>` element.

`angle`

The cross-sectional shape of the conductor is specified as trapezoidal. This attribute specifies the angle of the trapezoid.

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Figure 47 shows various trapezoidal cross-sectional shapes of the conductor.

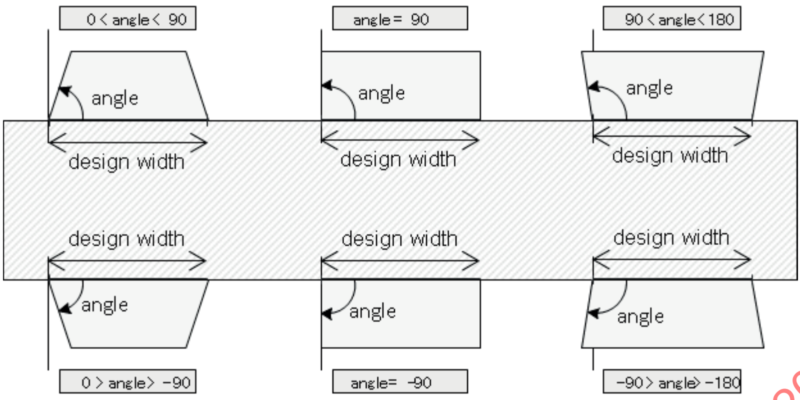

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Figure 47 —Explanatory drawing of trapezoidal angles

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9.2.13.4.3 Example

The following is an example of the <trapezoidal_angle> element in use.

```
<trapezodial_angle layer="L1" angle="60"/>
<trapezodial_angle layer="L4" angle="-60"/>
```

9.2.13.5 The <surface_roughness> element

9.2.13.5.1 General

The <surface_roughness> element specifies the roughness of the conductor surface.

```
<surface_roughness
             layer="layer_name"
             UP_RMS="up_rms"
             DOWN_RMS="down_rms"
/>
```

The <surface_roughness> element consists of the layer attribute, the `UP_RMS` attribute, and the `DOWN_RMS` attribute. Figure 48 shows the roughness of the conductor surface in root mean square (RMS).

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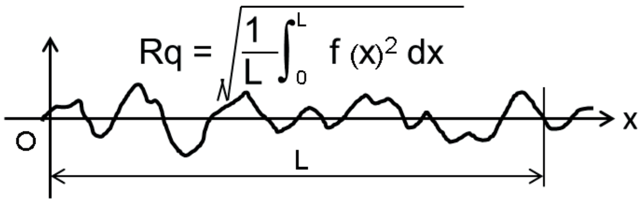

Rq: RMS deviation of the primary profile.

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Figure 48 — Explanatory drawing of surface roughness

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9.2.13.5.2 Attribute definitions

The attributes of the <surface_roughness> element are defined as follows:

`layer`

This attribute specifies the name of the conductor layer that is specified in the <layer_def> element.

`UP_RMS`

This attribute specifies the roughness of the top side surface of the conductor in RMS.

`DOWN_RMS`

This attribute specifies the roughness of the bottom side surface of the conductor in RMS.

Figure 49 shows `layer`, `UP_RMS`, and `DOWN_RMS` as attributes of the <surface_roughness> element.

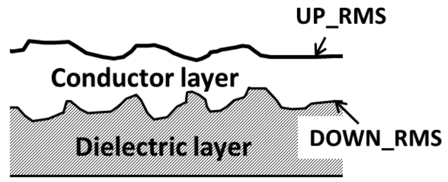

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Figure 49 — Explanatory drawing of `UP_RMS` and `DOWN_RMS`

9.2.13.5.3 Example

The following is an example of the <surface_roughness> element in use.

```
<surface_roughness layer="L1" UP_RMS="2" DOWN_RMS="5"/>
<surface_roughness layer="L4" UP_RMS="5" DOWN_RMS="2"/>
```

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9.3 The <Constraintrule> element

9.3.1 General

The <Constraintrule> element specifies the limited height of the component by the <height_limit> element and also specifies the non-default design rule area by the <design_rule_area> element.

```
<Constraintrule>
              [<height_limit> element]…
              [<design_rule_area> element]…
</Constraintrule>
```

The <Constraintrule> element consists of zero or more <height_limit> elements, and zero or more <design_rule_area> elements.

9.3.2 Element content

The <Constraintrule> element can contain the following elements:

```
<height_limit>
<design_rule_area>
```

9.3.3 Example

The following is an example of the <Constraintrule> element in use.

```
<Constraintrule>
    <height_limit>
        <top
            name="Top_Connector_Location"
            height="200"
            shape_id="Rec_6000um_8000um"
            x="3000" y="2000"
        />
        <bottom
            name="Bottom_Connector_Location"
            height="200"
            shape_id="Rec_6000um_8000um"
            x="3000" y="2000"
        />
    </height_limit>
    <design_rule_area
        ref_rule_name="C4_Area"
        shape_id="SQ_6000um_6000um"
        x="0" y="0"
    />
</Constraintrule>
```

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9.3.4 The <height_limit> element

9.3.4.1 General

The `<height_limit>` element specifies the limited height of the components from the surface of the top layer or bottom layer.

```
<height_limit>
              [<top> element]…
              [<bottom> element]…
</height_limit>
```

The `<height_limit>` element consists of zero or more `<top>` elements and zero or more `<bottom>` elements. Figure 50 shows the height limit of components from the surface of the top layer or bottom layer.

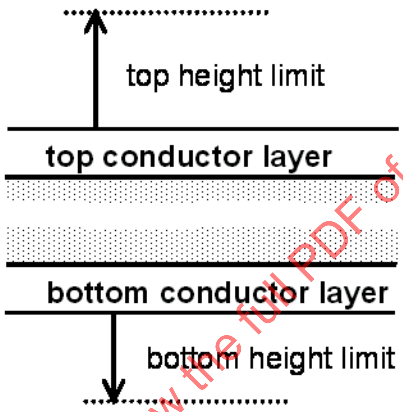

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Figure 50—Explanatory drawing of the top height limit and bottom height limit

9.3.4.2 Element content

The `<height_limit>` element can contain the following elements:

```
<top>
<bottom>
```

9.3.4.3 Example

The following is an example of the `<height_limit>` element in use.

```
<height_limit>
   <top
      name="Top_Connector_Location"
      height="200"
      shape_id="Rec_6000um_8000um"
      x="3000" y="2000"
   />
```

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```
   <bottom
       name="Bottom_Connector_Location"
       height="200"
       shape_id="Rec_6000um_8000um"
       x="3000" y="2000"
   />
</height_limit>
```

9.3.4.4 The <top> element

9.3.4.4.1 General

The <top> element specifies the maximum height for the placed components on the top layer.

```
<top
             name="area_name"
             height="height_limitation"
             shape_id="identifier_of_referenced_shape"
             x="x_coordinate"
             y="y_coordinate"
             [angle="rotation_angle"]
/>
```

The <top> element consists of the `name` attribute, the `height` attribute, the `shape_id` attribute, the `x` attribute, the `y` attribute, and the optional `angle` attribute.

9.3.4.4.2 Attribute definitions

The attributes of the <top> element are defined as follows.

`name`

This attribute specifies the name of the area that has a limited height on the top layer.

`height`

This attribute specifies the maximum height for the top layer.

`shape_id`

This attribute specifies the identification number of the shape that has the specified height-restricted space on the top layer. The origin coordinate of the shape coincides with the origin coordinate of the height-restricted space.

`x`

This attribute specifies the x-coordinate of origin in the height-restricted area.

`y`

This attribute specifies the y-coordinate of origin in the height-restricted area.

`angle`

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This attribute specifies the angle of the counterclockwise rotation with respect to the local origin. If it is not specified, zero is set as the default.

9.3.4.4.3 Example

The following is an example of the <top> element in use.

```
<top
    name="Top_Connector_Location"
    height="200"
    shape_id="Rec_6000um_8000um"
    x="3000" y="2000"
/>
```

9.3.4.5 The <bottom> element

9.3.4.5.1 General

The <bottom> element specifies the maximum height for the placed components on the bottom layer.

```
<bottom
                name="area_name"
                height="height_limitation"
                shape_id="identifier_of_referenced_shape"
                x="x_coordinate"
                y="y_coordinate"
                [angle="rotation_angle"]
/>
```

The <bottom> element consists of the `name` attribute, the `height` attribute, the `shape_id` attribute, the `x` attribute, the `y` attribute, and the optional `angle` attribute.

9.3.4.5.2 Attribute definitions

The attributes of the <bottom> element are defined as follows.

`name`

This attribute specifies the name of the area that has a limited height on the bottom layer.

`height`

This attribute specifies the maximum height for the bottom layer.

`shape_id`

This attribute specifies the identification number of the shape that has the specified height-restricted space on the bottom layer. The origin coordinate of the shape coincides with the origin coordinate of the height-restricted space.

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`x`

This attribute specifies the x-coordinate of origin in the height-restricted area.

`y`

This attribute specifies the y-coordinate of origin in the height-restricted area.

`angle`

This attribute specifies the angle of the counterclockwise rotation with respect to the local origin. If it is not specified, zero is set as the default.

9.3.4.5.3 Example

The following is an example of the `<bottom>` element in use.

```
<bottom
    name="Bottom_Connector_Location"
    height="200"
    shape_id="Rec_6000um_8000um"
    x="3000" y="2000"
/>
```

9.3.5 The <design_rule_area> element

9.3.5.1 General

The `<design_rule_area>` specifies the particular area that has the non-default design rules.

```
<design_rule_area
                ref_rule_name="name_of_referenced_design_rule"
                shape_id="identifier_of_referenced_shape"
                x="x_coordinate"
                y="y_coordinate"
                angle="rotation_angle"
/>
```

The default design rules in this area are overridden by the non-default design rules. It is possible to specify the different rules from the default design rules in `<design_rule_area>`, but it is impossible to specify the layer stackup locally. Even if the local design rule includes the statement that defines the layer structure, the definition will be ignored. The `<design_rule_area>` element consists of the `ref_rule_name` attribute, the `shape_id` attribute, the `x` attribute, the `y` attribute, and the optional `angle` attribute. Figure 51 shows the relationship between the default design rule area and the non-default design rule area.

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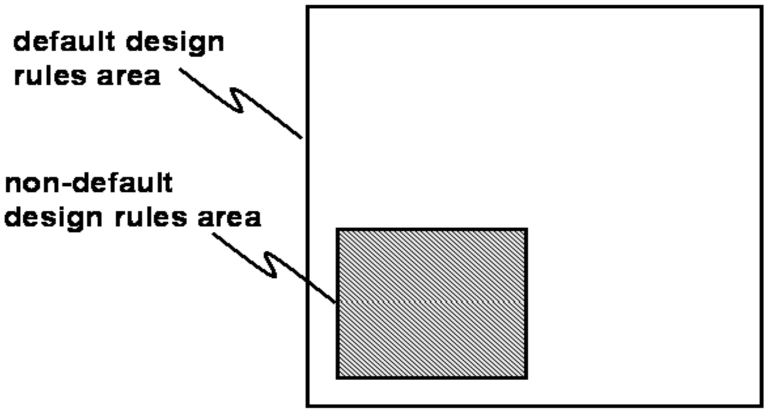

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Figure 51 —Explanatory drawing of the relationship of the default design rule area and the non-default design rule area

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9.3.5.2 Attribute definitions

The attributes of the `<design_rule_area>` element are defined as follows.

`ref_rule_name`

This attribute specifies the name of the predefined physical design rule that is used in the non-default design rule area. The physical design rule is specified in the `<Physicaldesign>` element.

`shape_id`

This attribute specifies the identification number of the shape that is specified in the non-default design rule area. The origin coordinate of the shape coincides with the origin coordinate of the area.

`x`

This attribute specifies the x-coordinate of origin.

`y`

This attribute specifies the y-coordinate of origin.

`angle`

This attribute specifies the angle of the counterclockwise rotation with respect to the local origin. If it is not specified, zero is set as the default.

9.3.5.3 Example

The following is an example of the `<design_rule_area>` element in use.

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```
<design_rule_area
    ref_rule_name="C4_Area"
    shape_id="SQ_6000um_6000um"
    x="0" y="0"
/>
```

10. N-Format

10.1 Purpose of the N-Format file

The N-Format file includes not only the signal connection but also the power/ground network. The N-Format file conforms to Verilog-HDL (IEEE Std 1364).

10.2 How to identify the power/ground network

Add the `/* PG_NET */` keyword at the power/ground port/wire definition as follows:

a) The port direction for power/ground is `inout`.

b) The net attribute of the power/ground is `wire`, not `supply0` or `supply1`.

c) Add the `/* PG_NET */` keyword at the power/ground port.

10.3 Example

The following is an example of the N-Format in use.

```
module XXXX ( VDD , VSS )
        inout VDD ; /* PG_NET */
        inout VSS ; /* PG_NET */
module YYYY ( ,, )
        wire VDD ;
        wire VSS ;
```

11. G-Format

11.1 Language basics of G-Format

11.1.1 Typographic and syntax conventions

This subclause describes the conventions used in the syntax definitions of the LPB G-Format.

`text`

The `monospace` and **bold** font is used to indicate the attributes or elements that shall be typed literally.

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italic

The *italic* font is used to indicate the user-defined information for which shall be substituted a name or value.

|

Vertical bars separate possible choices for a single attribute or element. They take precedence over any other character.

[ ]

Brackets denote optional attributes or elements. When used with vertical bars, they enclose a list of choices.

…

Three dots indicate that the previous value could be repeated.

Note that all of the strings in G-Format are treated as case sensitive.

NOTE—All code examples in this standard are written in monospace font.

11.1.2 Reserved Characters

#	If the first character of a line is a pound (#) sign, the line is ignored so it can be used for comments.
" "	Any data between two double quotation marks are considered as a string.

11.2 Structure

The G-Format file consists of several sections. Each section starts with a dot (.) followed by a keyword. The **`.version`**, **`.unit`**, and **`.scale`** sections consist of one line each. All other sections end with **`.end`** followed by the same keyword. The keyword in the **`.end`** line can be omitted. The header section consists of the **`.version`**, **`.unit`**, and **`.scale`** sections. Except for the **`.version`** section, any section can be omitted. The sections of the G-Format file are as follows:

`.version` *x y*

`.unit` [**`inch`** | **`mm`**]

`.scale` *value*

`.material`
definition
`.end` [**`material`**]

`.layer`
definition
`.end` [**`layer`**]

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```
.shape
definition
.end [shape]

.board_geom
definition
.end [board_geom]

.padstack
definition
.end [padstack]

.part
definition
.end [part]

.component
definition
.end [component]

.netattr
definition
.end [netattr]

.netlist
definition
.end [netlist]

.via
definition
.end [via]

.bondwire
definition
.end [bondwire]

.route
definition
.end [route]
```

11.3 Header section

11.3.1 General

The header section consists of the **.version**, **.unit**, and **.scale** sections.

. **version** *x y*

This section specifies a version of the G-Format file; *x* is a major version number; *y* is a minor version number. The **.version** section shall appear before any other section in the file.

x integer
y integer

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.unit *value*

This section specifies a geometric unit used throughout the G-Format file. The value shall be either **inch** or **mm**. If this section or the value is omitted, **inch** is assumed as the default.

value **inch** or **mm**

.scale *value*

This section specifies a geometric scale used throughout the G-Format file. The actual dimension of the data in the file is determined by dividing the number by the scale value. For example, if the unit is set to **inch** and the scale is 1000, the geometric data are in mils or 1/1000 in. If the unit is set to mm and the scale is 1000, the geometric data are in microns or micrometers. The default is **1**.

value iteger

11.3.2 Example

The following is an example of the header section of a G-Format file.

```
.version 1 0
.unit mm
.scale 1000
```

11.4 Material section

11.4.1 General

The **.material** section consists of the following:

.material
definition
.end [**material**]

This is an optional section giving material properties. List materials used in the design and their properties. Each material is defined as follows:

C *materialName conductivity*
or
D *materialName permittivity permeability lossTangent*
where

C or **D**	**C** stands for conducting material
	D stands for dielectric material
materialName	is the name of the material enclosed by double quotation marks
conductivity	is the electric conductivity (1/Ω mm)
permittivity	is the relative permittivity or dielectric constant
permeability	is the relative permeability
lossTangent	is the dielectric loss tangent

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11.4.2 Example

The following is an example of a **.material** section.

```
.material
D "AIR" 1.0 1.0 0.0
C "COPPER" 59000
C "GOLD"45500
D "FR-4" 4.5 1.0 0.035
D "SR" 4.3 1.0 0.03
.end material
```

11.5 Layer section

The **.layer** section consists of the following:

.layer
definition
.end [**layer**]

This section describes a layer stackup from top to bottom (or from front to back). Each layer is defined as follows:

name thickness type conducting dielectric1 [*dielectric2 dielectric3*]

where

name — is the name of the layer enclosed by double quotation marks. If unknown, write `""`.

thickness — is the thickness of the layer. If unknown, write **0**.

type — is the type of the layer, defined by a single character:
- **S** for signal layer
- **D** for dielectric layer
- **P** for power or ground layer if it can be differentiated from the signal layer

conducting — is the name of the conducting material entered as a string enclosed by double quotation marks.

dielectric1 — is the name of the dielectric material entered as a string enclosed by double quotation marks.

Note that throughout the G-Format File, signal layer numbers are the numbers that are numbered sequentially from the top by counting only the signal/power/ground layers.

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11.6 Shape section

11.6.1 General

The **.shape** section consists of the following:

.shape
definition
.end [**shape**]

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This section defines shapes that are referenced from other sections in the same file. Available shapes are polygon, rectangle, square, circle, annular, oblong, finger, bullet, and composite.

Each shape is defined as

id keyword parameters

where the *id* is a number that will be referenced by others and is sequentially numbered from 1. The *keyword* and *parameters* are described as follows.

id **`polygon {`** *x1 y1 x2 y2 …* **`}`**

Vertices of polygon shape (see Figure 52) are enclosed by `{ }`. Data can be shown on more than one line. The last point does not need to be the same as the first point. The reference point is at (0, 0).

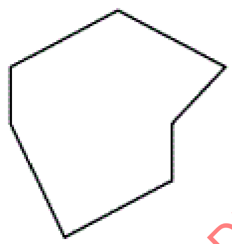

Figure 52—polygon

id **`rectangle`** *width height*

Each rectangle is defined by *width* and *length*. The definition shall appear on one line. The reference point is at the center of the rectangle. Figure 53 marks the reference point as X.

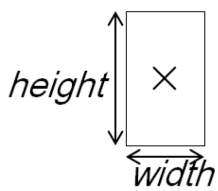

Figure 53—rectangle

id **`square`** *width*

Each square is defined by *width*. The definition shall appear on one line. The reference point is at the center of the square. Figure 54 marks the reference point as X.

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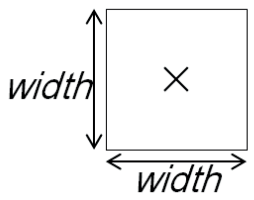

Figure 54—square

id **`circle`** *diameter*

Each circle is defined by *diameter*. The definition shall appear on one line. The reference point is at the center of the circle. Figure 55 marks the reference point as X.

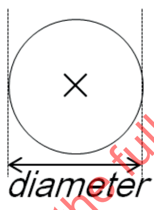

Figure 55—circle

id **`annular`** *outerDiem innerDiem*

Each donut is defined by *outerDiem* and *innerDiem*. The definition shall appear on one line. The reference point is at the center of the annular. Figure 56 marks the reference point as X.

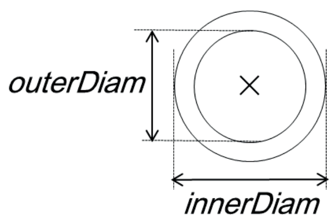

Figure 56—annular

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id **`oblong`** *width left right*

Each oblong is defined by *width*, *left*, and *right*. The definition shall appear on one line. The reference point is shown in Figure 57 marked as X.

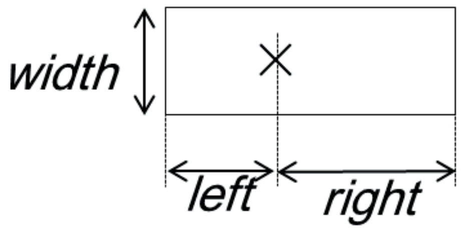

Figure 57—oblong

id **`bullet`** *width left right*

Each bullet is defined by *width, left*, and *right*. The definition shall appear on one line. The reference point is shown in Figure 58 marked as X.

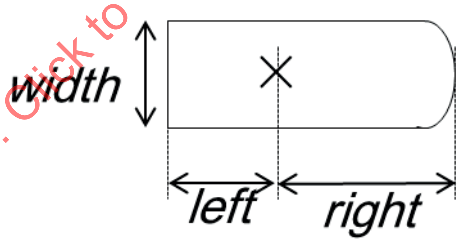

Figure 58—bullet

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id **finger** *width left right*

Each finger is defined by *width*, *left*, and *right*. The definition shall appear on one line. The reference point is shown in Figure 59 marked as X.

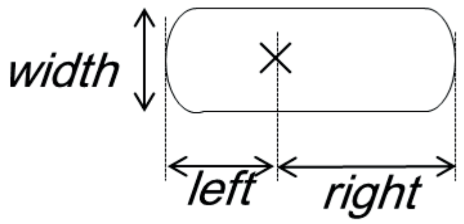

Figure 59—finger

id **composite {** *1st_point_segment1 segment2 …* **}**

A composite shape consists of lines and/or arcs. The definition is enclosed by **{ }** and can be shown on more than one line. There are four types of segments: straight line, clockwise arc (**arc**), counterclockwise arc (**rarc** or reverse arc), and an arc defined by three points (**arc3**).

No keyword between two points indicates that they are connected by a straight line. A keyword **arc, rarc**, or **arc3** between two points indicates that they are connected by a clockwise arc, a counterclockwise arc, or a three-point method arc, respectively. For **arc** and **rarc**, an arc origin appears after the arc end point. For **arc3**, a middle point appears after the arc end point.

The composite shape shown in Figure 60 can be described as

> *2* **composite {***xa ya xb yb xc yc* **rarc** *xd yd xp yp xe ye xf yf* **arc** *xg yg xq yq xh yh* **arc3** *xi yi xr yr***}**

where the *2* at the beginning is a shape identifier. The shape is made of straight lines *a*-*b* and *b*-*c*, then a counterclockwise arc from *c* to *d* with an origin at *p*, then straight lines *d*-*e* and *e*-*f*, then a clockwise arc from *f* to *g* with an origin at *q*, then straight line *g*-*h* and a three-point method arc from *h* to *i* with a middle point at *r*. Finally, the straight line from *i* to *a* is not defined because a straight line will connect the last point to the first point by default.

The same shape can also be described as:

> *2* **composite {***xa ya xi yi* **arc3** *xh yh xr yr xg yg* **rarc** *xf yf xq yq xe ye xd yd* **arc** *xc yc xp yp xb yb***}**

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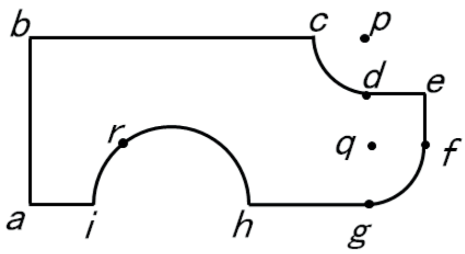

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Figure 60—composite

11.6.2 Example

The following is an example of a **.shape** section.

```
.shape
1 circle 50
2 circle 80
3 circle 300
4 rectangle 400 400
5 rectangle 700 5600
6 circle 750
7 composite {
          275 -200
          275 200
          -275 200
          -275 -200
}
8 composite {
          400 -100
          400 100
          -400 100
          -400 -100
}
.end shape
```

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11.7 Board geometry section

11.7.1 General

The **.board_geom** section consists of the following:

.board_geom
definition
.end [**board_geom**]

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The exterior geometry of a board or package is defined by one of the following four methods:

> **polygon {** *x1 y1 x2 y2 …* **}**
> **composite {** *1st_point_segment1 segment2 …* **}**
> **shape** *shapeID x y rotation mirror*
> **shape** *shapeID x y mirror rotation*

The methods for defining **polygon** and **composite** are the same as those described in the .shape section (11.6).

The **shape** is placed by defining the *shapeID*, the x and y coordinates (global coordinates) of the shape origin (local origin), the counterclockwise rotation in degrees, and the mirror indicator. Mirror indicators are as follows:

X mirror about X-axis
Y mirror about Y-axis
N no mirror

If the mirror indicator appears after the rotation, the mirror is performed after the rotation. If the mirror indicator appears before the rotation, the mirror is performed before the rotation.

Both mirror and rotation operations are performed with respect to the shape origin (local origin).

Holes (cutouts or voids) are defined by using one or more of the following methods.

> **void_polygon {** *x1 y1 x2 y2 …* **}**
> **void_rectangle** *width length x y*
> **void_square** *width x y*
> **void_circle** *diameter x y*
> **void_composite {** *1st_point_segment1 segment2 …* **}**
> **void_shape** *shapeID x y rotation mirror*
> **void_shape** *shapeID x y mirror rotation*

The **void_polygon**, **void_composite**, and **void_shape** are defined in the same way as for the **polygon**, **composite**, and **shape**, respectively.

The **void_rectangle**, **void_square**, and **void_circle** are defined in the same way as the **rectangle**, **square**, and **circle** are defined in the **.shape** section (11.6). They are placed at the coordinates *x* and *y*.

11.7.2 Example

The following is an example of a **.board_geom** section.

```
.board_geom
polygon {
          -50000 -40000
          50000 -40000
          50000 40000
          -50000 40000
}
.end board_geom
```

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11.8 Padstack section

11.8.1 General

The **.padstack** section consists of the following:

.padstack
definition
.end [**padstack**]

This section defines padstacks. Each padstack is defined as

padstackID **{** *pad1 pad2* ….**}**

where the *padstackID* is a number that will be referenced by vias in the **.via** section (11.13). The section is sequentially numbered from 1. As described below, pads are defined only by using the predefined shapes in the **.shape** section:

signalLayerNum shapeID shapeROT [apshapeID *apshapeROT*]

where

signalLayerNum	is the signal layer number as it appeared in the layer section.
shapeID	is the shape identifier.
shapeROT	is the counterclockwise rotation angle of the shape in degrees.
apshapeID	the anti-pad shape identifier. The anti-pad definition is optional.
apshapeROT	is the counterclockwise rotation angle of the anti-shape in degrees.

11.8.2 Example

The following is an example of a **.padstack** section.

```
.padstack
1 {
           1 3 0 4 0
           2 3 0 4 0
           3 3 0 4 0
           4 3 0 4 0
}
2 {
           1 3 0 4 0
           2 3 0 4 0
}
3 {
           2 3 0 4 0
           3 3 0 4 0
           4 3 0 4 0
}
4 {
           1 12 0
}
5 {
           1 13 0
}
6 {
           1 14 0
}
.end padstack
```

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11.9 Part section

11.9.1 General

The **.part** section consists of the following:

.part
definition
.end [**part**]

This section describes a part. Each part is defined as

partName [*shape llx lly urx ury height* [*type value* [**noflip**] [*material*]]] **{***pin1 pin2* ….**}**

where *partName* is the name of the part and *shape*, *llx*, *lly*, *urx*, *ury*, *height* and **noflip** are optional. If the keyword **noflip** appears, the part will not be flipped when it is placed below the layer.

partName	is the name of the part.
shape	is the top view shape of the part: **R** for rectangle **C** for circle
llx, *lly*	are the lower left coordinates of the bounding box.
urx, *ury*	are the upper right coordinates of the bounding box.
height	is the height.
type	is the part type: **R** for resistor **L** for inductor **C** for capacitor **S** for solder balls **D** for die **M** for molding compound **O** for other types
value	is the part value (mΩ for a resister, nH for an inductor, pF for a capacitor). Set it to zero for all other part types. If the three values are in parentheses **( )**, the part values are for a resistor, inductor, and capacitor; for example, (20.0 5 3.5).
material	is optional. The name of the material is enclosed by **" "**.

Pins are defined as

pinName x y ioType [*padstackID*]

where

pinName	is the name of the pin. If the name is not known, a sequential number will be used as a name.
x y	is the location of the pin with respect to local origin.
ioType	is the pin I/O type: **D** for driver pin **R** for receiver pin **B** for bidirectional pin **DT** for driver terminator **RT** for receiver terminator
padstackID	is optional. It is the padstack identifier (0 if the padstack is unknown).

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11.9.2 Example

The following is an example of a **`.part`** section.

```
CAP0603B R -300 -150 300 150 400 C {
           1 -425 0 B 23
           2 425 0 B 23
}
CAP1005B R -650 -250 650 250 400 C {
           1 -500 0 B 24
           2 500 0 B 24
}
REGULATOR R -2000 -2000 2000 2000 0 D {
           1 -1800 1050 B 21
           10 1800 -350 B 21
           11 1800 350 B 21
           12 1800 1050 B 21
           13 1050 1800 B 21
           14 350 1800 B 21
           15 -350 1800 B 21
           16 -1050 1800 B 21
           2 -1800 350 B 21
           3 -1800 -350 B 21
           4 -1800 -1050 B 21
           5 -1050 -1800 B 21
           6 -350 -1800 B 21
           7 350 -1800 B 21
           8 1050 -1800 B 21
           9 1800 -1050 B 21
}
SMA_X1 R -2750 -2750 2750 2750 0 O {
           1 0 0 B 18
           2 -2000 2000 B 18
           3 -2000 -2000 B 18
           4 2000 -2000 B 18
           5 2000 2000 B 18
}
.end part
```

11.10 Component section

11.10.1 General

The **`.component`** section consists of the following:

`.component`
definition
`.end` [**`component`**]

This section describes a component placement. One component placement appears per line. Each placed component is defined as:

U-name partName x y layer rotation [*stackComp*] [(*R L C 0*)]

where

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U-name	is the U-name, also known as the location identifier or reference designator. No space is allowed in the name.
partName	is the part name. The name is enclosed by double quotation marks (`" "`).
x y	is the location of the component origin with respect to the board origin.
layer	is the placement layer number: **+*n*** for above the layer **-*n*** for below the layer
rotation	is the counterclockwise rotation of the component in degrees with respect to the component origin (local origin).
stackComp	is optional. It is the name of the component on which this component is stacked. If this is defined, the layer number is ignored.
R L C 0	is optional. It is the component's R, L, C, and other values in a pair of parentheses; for example, (50 10 250 0). The units are mΩ, nH, or pF. The fourth value is for future use.

11.10.2 Example

The following is an example of a **`.component`** section.

```
.component
C10 CAP0603B -8584.7 -4104.9 -4 0
C11 CAP0603B -8584.7 -6355.9 -4 0
REGULATOR REGULATOR -12598 10183.9 1 0
SMA_X1 SMA_X1 1570.7 32293.2 1 0
SMA_X2 SMA_X1 -7429.3 32293.2 1 0
.end component
```

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11.11 Net attribute section

The **`.netattr`** section consists of the following:

`.netattr`
definition
`.end` [**`netattr`**]

This section defines net attributes, such as net class, allowable delays, and other user properties.

Each attribute group is defined as

id **{***attrributeName1***=***value1 attributeName2***=***value2* ….**}**

where the *id* is an attribute group number that will be referenced by nets in the netlist section and is sequentially numbered from 1. More than one attribute can be defined for one group. Each attribute group definition can appear on more than one line. Attribute assignments appear in the braces **{ }**. Each attribute assignment consists of *attributeName*, an equals sign (=), and the *value*.

11.12 Netlist section

11.12.1 General

The **`.netlist`** section consists of the following:

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```
.netlist
definition
.end [netlist]
```

This section defines netlists. Each net is defined as

netName netType attributeID {*node1 node2* ….}

where

netName	is the net name.
netType	is the net type: **S** for signal net (**s** if broken) **P** for power net (**p** if broken) **G** for ground net (**g** if broken)
attributeID	is the net attribute identifier. Zero indicates that the attribute is unknown.

Each node is defined as

U-name pinNumber ioType [**{***x y layer***}**]

where

U-name	is the U-name. A minus sign (-) indicates an unknown U-name.
pinNumber	is the pin number or pin name.
ioType	is the pin I/O type: **D** for driver pin **R** for receiver pin **B** for bidirectional pin **DT** for driver terminator **RT** for receiver terminator A placeholder minus sign (-) shall appear if the type defined for the pin in the part section is to be used.
x y	is the location of the pin origin with respect to the board origin.
layer	is the placement layer number.

The pin location can appear at the end of the node definition. It is optional and shall be enclosed by **{ }**. Set the layer number to negative for solder balls.

11.12.2 Example

The following is an example of a **.netlist** section.

```
.netlist
"FKOUT[2]" S 0 {
           FKB48 M1 B
           SMA_X4 1 B
}
"N1" S 0 {
           XTAL 3 B
           MCR1_R7 B B
           MCR1_R8 B B
           GRM1_C2 A B
}
"PCIREFCLK_N" S 0 {
```

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```
            SOC AE12 B
            PCIE A14 B
}
"PCIREFCLK_P" S 0 {
            SOC AF12 B
            PCIE A13 B
}
"PCITR0_N" S 0 {
            SOC AE14 B
            PCIE A17 B
}
.end netlist
```

11.13 Via section

11.13.1 General

The **.via** section consists of the following:

.via
definition
.end [**via**]

This section defines vias. One via definition appears per line. Each via is defined as

viaName padstackID padstackROT shapeID shapeROT [*thickness*]

where

viaName	is the via name that will be referenced by routing in the route section.
padstackID	the padstack identifier. Zero indicates that no padstack exists for the via.
padstackROT	is the counterclockwise rotation angle of the padstack.
shapeID	is the shape identifier of the via barrel.
shapeROT	is the counterclockwise rotation angle of the via barrel shape.
thickness	is optional. It is the thickness of the via barrel wall. If the thickness is 0, the via barrel is filled by material (see Figure 61).

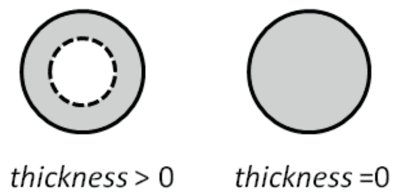

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Figure 61 —via

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11.13.2 Example

The following is an example of a **.via** section.

```
.via
VIA14 1 0 2 0
VIA12 2 0 2 0
VIA24 3 0 2 0
VIA13 4 0 2 0
VIA14B 18 0 17 0
.end via
```

11.14 Bondwire section

11.14.1 General

The **.bondwire** section consists of the following:

.bondwire
definition
.end [**bondwire**]

This section defines bond wire geometry. One bond wire definition appears per line. Each bond wire is defined as

id type material diameter hw hd alpha beta [*profile_name*]

where the *id* is a number that will be referenced by routing in the route section and is sequentially numbered from 1. As illustrated in Figure 62 and Figure 63,

type is the bond wire type:
- **D** for die-down configuration
- **U** for die-up configuration

material is the material name or electric conductivity (1/Ω mm). If it is a name, it shall be enclosed by double quotation marks (" ").

diameter is the wire diameter.

hw is the wire loop height.

hd is the die height:

$H_{die\_pad} - H_{top\_of\_top\_metal\_layer}$ for die-up

$H_{die\_pad} - H_{bottom\_of\_bottom\_metal\_layer}$ for die-down

alpha is the die side angle in degrees.

beta is the package substrate side angle in degrees.

profile_name is the name of the bond wire profile associated with the *id*.

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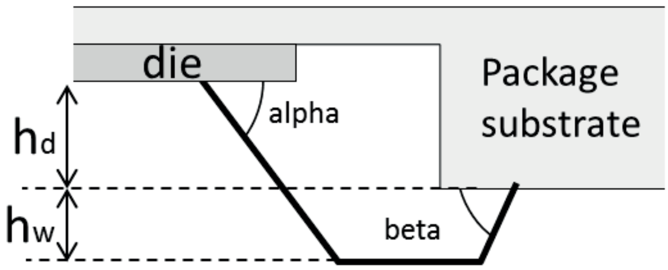

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Figure 62—Die-down configuration

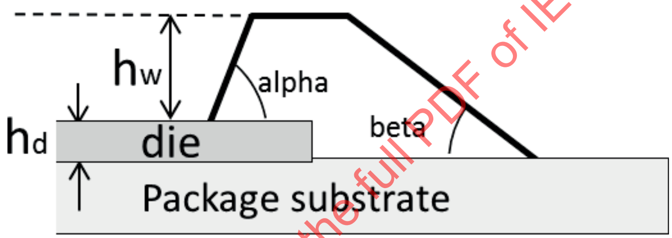

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Figure 63—Die-up configuration

11.14.2 Example

The following is an example of a **`.bondwire`** section.

```
.bondwire
1 U "GOLD" 20 70 290 60 20 innerwire
2 U "GOLD" 20 140 290 60 40 outerwire
.end bondwire
```

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11.15 Route section

11.15.1 General

The **.route** section consists of the following:

.route
definition
.end [**route**]

This section defines routed nets. Each routed net is defined as

netName **{** *segment1 segment2* ….**}**

where *netName* is one of the nets that appeared in the **.netlist** section. Each routed net consists of one or more segments. Each segment is defined by one of the following methods. All of these methods are in the form of

segment_type signal_layer_number(s) segment_definition
path *layer width* **{** *1st_point_segment1 segment2* … **}**
via *beginLayer endLayer viaName x y rotation [mirror]*
bondwire *beginLyr endLyr bondwireID xb yb xe ye [die1 die2]*
polygon *layer* **{** *x1 y1 x2 y2* …**}**
rectangle *layer width length x y*
square *layer width x y*
circle *layer diameter x y*
annular *layer outerDiem innerDiem x y*
composite *layer* **{** *1st_point_segment1 segment2* … **}**
shape *layer shapeID x y rotation mirror*
shape *layer shapeID x y mirror rotation*
void_polygon *layer* **{** *x1 y1 x2 y2* …**}**
void_rectangle *layer width length x y*
void_square *layer width x y*
void_circle *layer diameter x y*
void_composite *layer* **{** *1st_point_segment1 segment2* … **}**
void_shape *layer shapeID x y rotation mirror*
void_shape *layer shapeID x y mirror rotation*

The **path** segment is defined the same way that the **composite** shape is defined in the **.shape** section, except that it has a *width* and the last point does not automatically connect to the first point.

The **via** segment requires *beginLayer* and *endLayer* numbers, while other segments require only one layer number. The via segment also requires the following:

viaName	name of the via defined in the via section
x y	location of the via
rotation	counter-clockwise rotation angle of the pad stack in degrees
mirror	optional; padstack mirror flag: **Y** mirror padstack **N** do not mirror padstack

The **bondwire** segment requires the following:

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beginLyr	Signal layer number of a beginning point. In order to indicate a die, enter a negative wire group identifier.
endLyr	Signal layer number of an ending point. In order to indicate a die, enter a negative wire group identifier.
bondwireID	Bond wire identifier. (0 if unknown)
xb yb	Beginning point coordinate
xe ye	Ending point coordinate
die1 die2	Optional die component names. The name(s) appear here only if the *begin_lyr* and/or *end_lyr* are negative.

All other segment types are defined the same way as they are defined in the **.shape** section or in the **.board_geom** section.

11.15.2 Example

The following is an example of a **.route** section.

```
"AGND" {
        via 1 4 VIA14B -429.3 34293.2 0 N
        via 1 4 VIA14B -429.3 30293.2 0 N
        via 1 4 VIA14B -9429.3 34293.2 0 N
        shape 1 7 -24821.9 24278.3 0 N
        shape 1 12 -3779.3 23603.4 0 N
        composite 2 {
                -47360 23040
                -15983.4 23040
                -15360 22416.6
                -15360 18416.6
                -14960 18016.6
                -14960 13616.6
                -14783.4 13440
                -4640 13440
                -4640 22416.6
                -4016.6 23040
                6560 23040
                6560 35360
                -47360 35360
        }
        void_composite 2 {
                -41295.6 25636.1
                arc -40975.6 25636.1 -41135.6 25636.1
                arc -41295.6 25636.1 -41135.6 25636.1
        }
        path 1 80 {
                -7825.9 27607.5
                -6985.3 27607.5
        }
        path 1 80 {
                -4082.8 25942.8
                -4082.8 25683
        }
        path 1 80 {
                -3719.3 23633.2
                -3380.3 23633.2
        }
        path 1 80 {
                -7390.9 22442.4
                -7130.9 22442.4
        }
```

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```
}
"AVDD33" {
           shape 1 8 -12948 11983.9 90 N
           shape 1 7 -36821.9 23278.3 0 N
           shape 1 7 -34821.9 23278.3 0 N
           shape 1 7 -29821.9 24278.3 0 N
           composite 3 {
                         -42160 23040
                         -15183.4 23040
                         -14560 22416.6
                         -14560 15840
                         -12640 15840
                         -12640 24960
                         -38816.6 24960
                         -39040 25183.4
                         -39040 25760
                         -42160 25760
           }
           via 1 3 VIA13 -13451.3 16882.6 0 N
           via 1 3 VIA13 -36821.9 23278.3 0 N
           via 1 3 VIA13 -24821.9 23278.3 0 N
           shape 1 11 -13457.1 16897.2 270 N
           shape 1 11 -41161.1 25621.3 0 N
           via 1 4 VIA14 -41135.6 25636.1 0 N
}
"DDRAD[0]" {
           shape 1 9 10900 0 0 N
           shape 1 6 34806.5 -1623.2 0 N
           shape 1 6 34547.6 17511.7 0 N
           shape 1 14 26777.7 18269.6 0 N
           via 1 4 VIA14 34200 2360 0 N
           via 1 4 VIA14 34226.5 635 0 N
           via 1 4 VIA14 33967.6 19939 0 N
           path 1 80 {
                         33967.6 19939
                         33967.6 19661.7
                         33967.6 19508.4
                         33977.6 19498.4
                         33977.6 18875.6
                         34057.6 18795.6
                         34057.6 18577.3
                         34137.6 18497.3
                         34137.6 18279.1
                         34187.6 18229.1
                         34187.6 18162.6
                         34547.6 17802.6
                         34547.6 17511.7
           }
           path 4 80 {
                         34200 2360
                         34200 2904
                         34170 2934
                         34170 11978
                         34157.6 11990.4
                         34157.6 12769.6
                         33967.6 12959.6
                         33967.6 19939
           }
           path 1 80 {
                         34226.5 635
                         34226.5 526.8
                         34226.5 373.5
                         34236.5 363.5
```

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```
                        34236.5 -259.3
                        34316.5 -339.3
                        34316.5 -557.5
                        34396.5 -637.5
                        34396.5 -855.8
                        34446.5 -905.8
                        34446.5 -972.3
                        34806.5 -1332.3
                        34806.5 -1623.2
          }
          path 4 80 {
                        34200 2360
                        34200 841.5
                        34226.5 815
                        34226.5 635
          }
          path 1 80 {
                        34200 2360
                        33650.8 2360
                        33568.5 2442.3
                        16116 2442.3
                        14003.7 330
                        13900 330
                        13870 360
                        11750.9 360
                        11390.9 0
                        10900 0
          }
}
.end route
```

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Annex A

(informative)

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Bibliographical references are resources that provide additional or helpful material but do not need to be understood or used to implement this standard. Reference to these resources is made for informational use only.

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[B10] IEC62433-5, EMC IC modeling – Part 5: Models of integrated circuits for EMI behavioural simulation – Radiated Immunity modelling (ICIM-RI).

[B11] XML Path Language (XPath) Version 1.0[10].

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[10] Available at http://www.w3.org/TR/xpath/

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Annex B

(informative)

Examples of utilization

B.1 Understanding the function of the LPB Format

This annex explains how and when the LPB Format is used in the design flow of an LSI, package, and board.

This annex contains the following:

1) Test bench
2) Design flow example
3) Growth of the sample files in the LPB Format
4) Simulations using the sample files in the LPB Format

This annex shows examples of the LPB Format, but parts are left out for want of space. Consecutive tildes (~~~) in the example code indicate that code has been omitted.

All examples of the LPB Format in this section are reprinted with permission from JEITA.

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B.2 Test bench

Figure B.1 shows the image of the test bench that will be developed using the LPB Format. This test bench contains the following

a) Custom LSI

   1) System on chip (SoC)

b) General purpose integrated circuit

   2) Double data rate 3 synchronous dynamic random-access memory (DDR3-SDRAM)
   3) Analog LSI
   4) Power integrated circuit (switching regulator)

c) Other parts

   5) Crystal (Xtal)
   6) Subminiature version A (SMA) ports
   7) Peripheral Component Interconnect Express (PCIe) Gen.2 port (Card edge finger)
   8) Resistor, capacitor etc.

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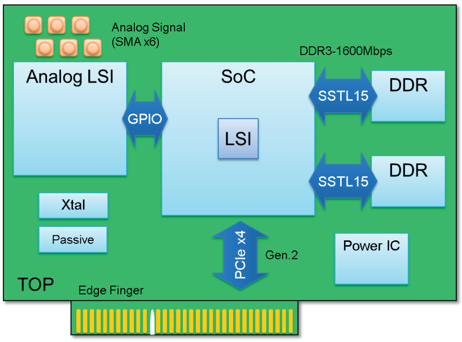

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Figure B.1—Image of the test bench

Figure B.2 is a use-case of the project to develop this test bench. The actors appearing in the project are as follows:

— **Electric products maker:** plans the development of this test bench and manages the project; designs the overall system.

— **LSI vendor:** will develop a custom LSI on order from the Electric Products Maker.

— **Printed-circuit-board (PCB) designer:** will design a printed circuit board on order from the Electric Products Maker.

— **Substrate/component vendors:** provide the general-purpose parts and the design rule of the printed circuit board for this project.

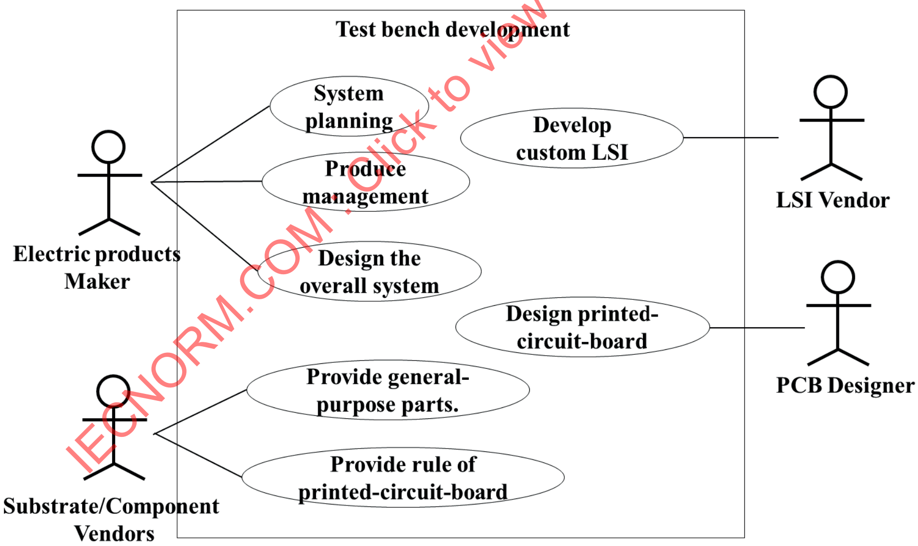

Figure B.2—Use-case of test bench development

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B.3 Design flow example

B.3.1 General

B.3.1.1 Example diagram

Figure B.3 shows an example of design using the LPB Format. Information described in the LPB Format is the input and output of each step in the design. The design results of each step in the design process are added to the LPB Format files. The files in LPB Format are exchanged between each of the LPB design sites in the design flow.

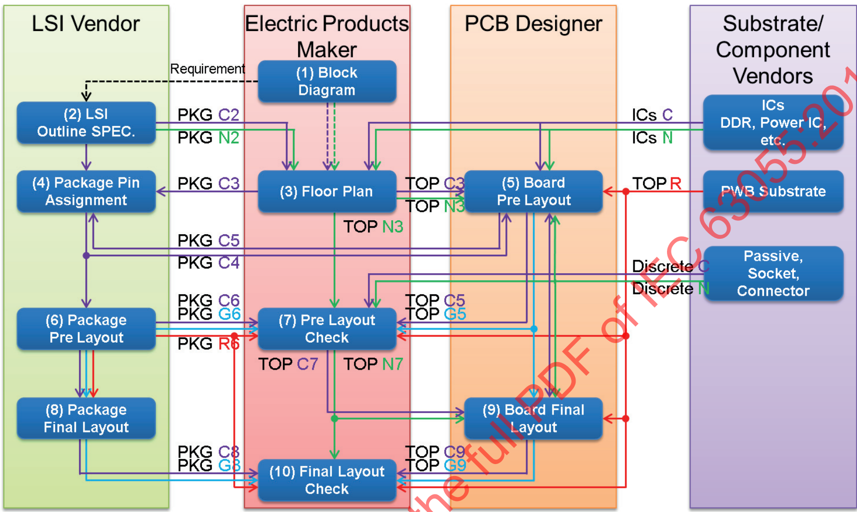

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Figure B.3—A design flow example using the LPB Format

B.3.1.2 General-purpose parts

Component vendors provide general-purpose parts to the electric products maker and PCB designer (see Figure B.4). They share the same information about the parts. The electronic products maker uses this information for system planning and verification; the PCB designer uses it for artwork design.

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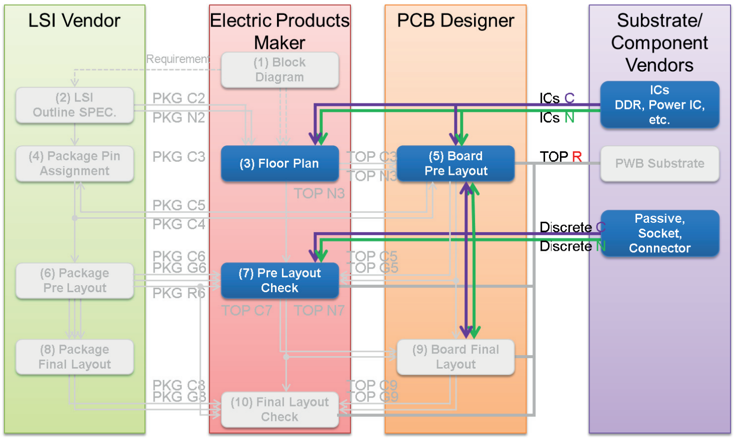

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Figure B.4—Providing general-purpose parts

The following code sections (List B.11 to List B.5) are examples of LPB Format files for DDR memory. They are composed of M-Format, C-Format, R-Format, and N-Format files and a Simulation Program with Integrated Circuit Emphasis (SPICE) model. C-Format defines the footprint of the package and design constraints. R-Format defines the three-dimensional shape of solder balls for the package. N-Format defines the input and output interface of the module. The SPICE file is a model of the power distribution network in DDR memory. M-Format manages those files.

List B.1 is an example of M-Format for DDR memory:

```
<?xml version="1.0" encoding="Shift_JIS"?>
<LPB_MFORMAT version="2.2" >
  <header
    project="LPB_2014_SAMPLE"
    design_revision="1.0"
    date="2015/03/20 13:00:00"
    author="Format SWG"
    company="JEITA"
  />
  <class comment="DDR Memory" >
    <CFORMAT comment="PKG" file_name="LPB2012CFMT_DDR.xml"
      design_revision="1.0"/>
    <RFORMAT   comment=""    file_name="LPB2012RFMT_DDR.xml"
      design_revision="1.0"/>
    <NFORMAT   comment=""    file_name="LPB2012NFMT_DDR.v"/>
    <OtherFile file_name="LPB2012_DDRPowerModel.sp"/>
  </class>
</LPB_MFORMAT>
```

List B.2 is an example of C-Format for DDR memory:

```
<?xml version="1.0" encoding="Shift_JIS"?>

<LPB_CFORMAT version="2.2" >
  <header
    project="LPB_2014_SAMPLE"
    design_revision="1.0"
    date="2015/03/20 13:00:00"
```

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```
    author="Format SWG"
    company="JEITA"
  />
  <global>
    <unit>
      <distance   unit="um" />
      <angle      unit="degree" />
      <frequency  unit="MHz" />
      <time       unit="ps" />
    </unit>
    <shape>
      <circle    id="SHAPE.10" diameter="200" />
      <rectangle id="SHAPE.21" width="7500" height="10900" />
    </shape>
    <padstack_def>
      <padstack id="PAD.10">
        <ref_shape shape_id="SHAPE.10" x="0" y="0" pad_layer="BOTTOM" />
      </padstack>
    </padstack_def>
  </global>

  <module name="DDR" type="PKG" shape_id="SHAPE.21" x="0" y="0">
    <socket  name="DDR" >
      <default>
        <port_shape padstack_id="PAD.10" />
        <ball_shape ball_name="DDRBALL" />
      </default>
      <port id="N1" x="-3200" y="-4800" name="VSS"
       direction="inout"  type="ground"/>
      <port  id="N2"  x="-2400"  y="-4800" name="RESET_N"
       direction="in"  type="signal"  />
      <port  id="N3"  x="-1600"  y="-4800" name="A[13]"
       direction="in"  type="signal"  />
      <port  id="N7"  x="1600"  y="-4800" name="A[14]"
       direction="in"  type="signal"  />
      <port  id="N8"  x="2400"  y="-4800" name="A[8]"
       direction="in"  type="signal"  />
      <port  id="N9"  x="3200"  y="-4800" name="VSS"
       direction="inout"  type="ground"  />
      <port  id="M1"  x="-3200"  y="-4000" name="VDDQ"
       direction="inout"  type="power"  />
      <port  id="M2"  x="-2400"  y="-4000" name="A[7]"
       direction="in"  type="signal"  />
      <port  id="M3"  x="-1600"  y="-4000" name="A[9]"
       direction="in"  type="signal"  />
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~

      <portgroup name="VDD">
              <ref_port  name="VDD"/>
              <ref_port  name="VDDQ"/>
      </portgroup>
      <portgroup name="VSS">
              <ref_port  name="VSS"/>
              <ref_port  name="VSSQ"/>
      </portgroup>
      <portgroup name="DATA">
              <ref_port  name="DM"/>
              <ref_port  name="DQ[7]"/>
              <ref_port  name="DQ[6]"/>
              <ref_port  name="DQ[5]"/>
              <ref_port  name="DQ[4]"/>
              <ref_port  name="DQ[3]"/>
              <ref_port  name="DQ[2]"/>
```

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```
            <ref_port  name="DQ[1]"/>
            <ref_port  name="DQ[0]"/>
    </portgroup>
   ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~

    <powerdomain_group port_name="VDDQ" typ="1.5">
      <ref_portgroup name="DATA" />
      <ref_portgroup name="DATASTROB" />
    </powerdomain_group>
    <powerdomain_group port_name="VSSQ" typ="0">
      <ref_portgroup name="DATA" />
      <ref_portgroup name="DATASTROB" />
    </powerdomain_group>
  ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~

    <swappable_port>
            <ref_port  name="DQ[7]"/>
            <ref_port  name="DQ[6]"/>
            <ref_port  name="DQ[5]"/>
            <ref_port  name="DQ[4]"/>
            <ref_port  name="DQ[3]"/>
            <ref_port  name="DQ[2]"/>
            <ref_port  name="DQ[1]"/>
            <ref_port  name="DQ[0]"/>
    </swappable_port>
    <constraint>
        <impedance group_name="CLOCK"   type="differential"
             min="95" typ="100" max="105" />
        <impedance group_name="DATASTROB"   type="differential"
             min="95" typ="100" max="105" />
        <impedance group_name="ADDRESS"     type="single"
            min="45" typ="50" max="55" />
  ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~

        <skew group_name="CLOCK"      min="2" max="2" />
        <skew group_name="DATASTROB"  min="2" max="2" />
    </constraint>
  </socket>

  <reference xmlns:spice="http://www.jeita.or.jp/LPB/spice"
              reffile="LPB2012_DDRPowerModel.sp" format="SPICE" >
    <connection socket_name="DDR" port_id="M9">
       <spice:ref_port subckt="DDRPowerModel" portid="1"/>
    </connection>
    <connection socket_name="DDR" port_id="K9">
       <spice:ref_port subckt="DDRPowerModel" portid="2"/>
    </connection>
    <connection socket_name="DDR" port_id="G2">
       <spice:ref_port subckt="DDRPowerModel" portid="3"/>
    </connection>
  ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~

  </reference>
 </module>
</LPB_CFORMAT>
```


List B.3 is an example of R-Format for DDR memory:


```
<LPB_RFORMAT version="2.2" >
  <header
    project="LPB_2014_SAMPLE"
    design_revision="1.0"
```


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```
    date="2015/03/20 13:00:00"
    author="Format SWG"
    company="JEITA"
  />
  <global>
    <unit>
      <distance    unit="um" />
      <resistivity unit="ohmm" />
    </unit>
  </global>
  <Physicaldesign name="footprint">
    <default/>
    <material_def>
        <conductor material="SOLDER"
             volume_resistivity="2.17e-7" temperature="20" />
    </material_def>
    <ball_def>
      <ball name="DDRBALL" material="SOLDER">
        <frustum height="250" diam1="300" diam2="600" />
        <frustum height="250" diam1="600" diam2="300" />
      </ball>
    </ball_def>
  </Physicaldesign>
</LPB_RFORMAT>
```

List B.4: An example of N-Format for DDR memory:

```
/*
 * 2013/03/06 : JEITA Sample N-Format file
 */
//-- DDR3 SDRAM -----------------------------------
module DDR ( A, BA, CAS_N, RAS_N, WE_N, CS_N, CKE, ODT, RESET_N,
             CK, CK_N,  DQS, DQS_N, DM, DQ, ZQ,
             VREFCA, VREFDQ, VDD, VSS, VDDQ, VSSQ );
  input [15:0] A ;
  input [2:0]  BA ;
  input CAS_N, RAS_N, WE_N, CS_N, CKE, ODT, RESET_N;
  input CK, CK_N ;
  input DQS, DQS_N ;
  input DM ;
  inout [7:0] DQ ;
  input ZQ ;
  inout VREFCA ;
  inout VREFDQ ;
  inout VDD ;     /* PG_NET */
  inout VSS ;     /* PG_NET */
  inout VDDQ ;    /* PG_NET */
  inout VSSQ ;    /* PG_NET */
endmodule
```

List B.5 is an example of a SPICE model that is referenced by C-Format:

```
*** LPB2012_DDRPowerModel.sp
.SUBCKT DDRPowerModel
+ VDD1  VDD2  VDD3  VDD4  VDD5  VDD6  VDD7
+ VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6
+ VSS1  VSS2  VSS3  VSS4  VSS5  VSS6  VSS7  VSS8 VSS9 VSS10 VSS11
+ VSSQ1 VSSQ2 VSSQ3 VSSQ4 VSSQ5 VSSQ6

C_VDD1 VDD1 0 5.00E-10
C_VDD2 VDD2 0 5.00E-10
```

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```
C_VDD3 VDD3 0 5.00E-10
C_VDD4 VDD4 0 5.00E-10
C_VDD5 VDD5 0 5.00E-10
C_VDD6 VDD6 0 5.00E-10
C_VDD7 VDD7 0 5.00E-10

C_VDDQ1 VDDQ1 0 3.00E-11
C_VDDQ2 VDDQ2 0 3.00E-11
C_VDDQ3 VDDQ3 0 3.00E-11
C_VDDQ4 VDDQ4 0 3.00E-11

~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
```

B.3.1.3 Design rule for the printed circuit board

The substrate vendor provides the design rule for the printed circuit board to the PCB designer and electric products maker (see Figure B.5). The PCB designer uses it for artwork layout. The electric products maker uses it for verification of the printed circuit board design.

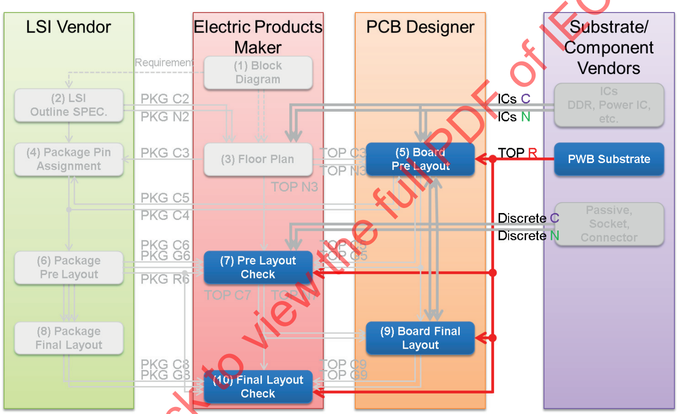

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Figure B.5—Providing the design rule for the printed circuit board

The following code section (List B.6) is an example of F-Format that is provided by the substrate vendor. It contains the following information:

— Shape of vias
— Electrical properties of the materials used for the printed circuit board
— Layer stackup of the printed circuit board
— Design rules, such as minimum line and space

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List B.6 is an example of R-Format for a printed circuit board:

```
<?xml version="1.0" encoding="Shift_JIS"?>
<LPB_RFORMAT version="2.2" >
  <header
    project="LPB_2014_SAMPLE"
    design_revision="1.0"
    date="2015/03/20 23:00:00"
    author="Format SWG"
    company="JEITA"
  />
  <global>
    <unit>
      <distance     unit="um" />
      <angle        unit="degree" />
    </unit>
    <shape>
       <circle id="ViaLand"   diameter="600"/>
       <circle id="ViaAnti"   diameter="900"/>
       <circle id="Drill"     diameter="300"/>
       <circle id="Hole"      diameter="260"/>
    </shape>
    <padstack_def>
       <padstack id="VIA14">
         <ref_shape shape_id="ViaLand" type="Land"    x="0" y="0" layer="L1"/>
         <ref_shape shape_id="ViaAnti" type="Antipad" x="0" y="0" layer="L1"/>
         <ref_shape shape_id="Drill"   type="Drill"   x="0" y="0" layer="L1"/>
         <ref_shape shape_id="Hole"    type="Hole"    x="0" y="0" layer="L1"/>
         <ref_shape shape_id="ViaLand" type="Land"    x="0" y="0" layer="L2"/>
         <ref_shape shape_id="ViaAnti" type="Antipad" x="0" y="0" layer="L2"/>
  ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~

       </padstack>
    </padstack_def>
  </global>

  <Physicaldesign name="DEFAULT_RULE">
    <default/>
    <material_def>
      <conductor material="Copper"
          volume_resistivity="1.7e-08" temperature="20.0" />
      <dielectric material="FR-4"   permittivity="4.37"
          tan_delta="0.01" frequency="1000" />
      <dielectric material="SR"     permittivity="4.3"
           tan_delta="0.03" frequency="1000" />
    </material_def>

    <layer_def>
       <layer name="Die1" type="dielectric"
        thickness="23" conductor_material="Copper" dielectric_material="SR"/>
       <layer name="L1" type="conductor" thickness="38" plate_thickness="20"
        conductor_material="Copper" dielectric_material="SR">
             <line_width min="500" max="5000"/>
             <area_limit min="22500" />
       </layer>
       <layer name="Die3" type="dielectric"
        thickness="200" conductor_material="Copper"
        dielectric_material="FR-4"/>
       <layer name="L2"    type="conductor" thickness="35"
        plate_thickness="0" conductor_material="Copper"
        dielectric_material="FR-4">
             <line_width min="500" max="5000"/>
```

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